University of California
Santa Barbara

On Wafer-Bonded Junctions and Transistors - Design, Fabrication, Challenges and Discoveries

A dissertation submitted in partial satisfaction
of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

Shalini Lal

Committee in charge:

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For my family and teachers who taught me to learn and unlearn.

Acknowledgements

It's important for me to acknowledge and thank the many teachers, mentors, family and friends who supported me in this journey.

In making me part of the wafer-bonding project Prof. Mishra gave me a ticket to a chance of a lifetime. He is many-things combined in one. Each interaction with him was a lesson in multiple themes, like ways to improve one's behavior, coming up with ideas, problem solving, keeping reasonable milestones, making hypothesis and assumptions, teaching, writing, presenting and explaining a phenomenon. I am grateful for this training which effectively modified my DNA and made me a better individual and researcher. Were it not for his prophetic acumen and unfailing ability of being able to nose out bad research habits, little progress would have been afforded in this dissertation. I would also like to thank him for all his contributions, his abilities of critiquing data and asking the right questions.

The training while TAing for Prof. Rodwell and Prof. Dagli served me in good stead and prepared me for Ph.D. program. I thank them for their support. I am also indebted to Professor Chris Van de Walle for his invaluable help in understanding the trap passivation mechanism.

I am exceedingly grateful to my committee members, who trained and made me part of their unorthodox styles and ideas. Their expertise not only identified the grey parts of the data, device physics, and understanding but also hinted on the way forward through it. Their feedback led to resorting to new ways of analysis and added consistency to the explanations. As a student I owe a lot of gratitude to them for their encouragement and to allow me to consider unorthodox ideas.

The dissertation required experimenting with cleanroom fabrication techniques - devising new recipes and modifying existing knowledge. The deficit of training and ideas in this area was overcome by the expertise of Brian Thibeault. His infinite knowledge combined with calm risk-taking ability and integrity is a rare combination. His contribution lies in creating many opportunities and eliminating challenges in process development of

wafer-bonded devices. In addition, the device physics and analysis owes a lot of its formation to the many discussions with him. Besides this, he helped me find a way through personal challenges for which I am grateful to him.

There were other mentors who helped and inspired the work in different aspects like mask designing, presentations, writing, measuring, understanding device characteristics and physics. For these I would like to thank Man Hoi, Uttam, Srabanti, Enrico, Geetak, Andy, Seshadri, Rob, Masataka and Nik.

It was a joy to work in cleanroom not only for its advanced setup but also because of the possibility of interacting and learning in the company of an experienced and exceptional staff. The cleanroom equipment would go down, samples would get damaged - there were challenges but one could feel the positives floating around in the form of the professionalism, encouragement, modesty and flexibility that the staff offered. I thank Don, Adam, Ning, Tony, Aidan, Bill, Brian L, Luis, Mike, Jack and Tom for their support.

Understanding and making wafer-bonded devices were not a one-person job. I am grateful to Eric, Nik and Erol who were very kind to share their bonding expertise and to Jeonghee who took the work to newer heights. I owe gratitude to another member of the team - BAVET (or wafer-bonded current aperture vertical electron transistor) as it provided a perfect medium to explore ones abilities and was the main source of surprises and perplexity that formed this work. No progress was possible if it were not for the roles played by each of the team members.

The team of Jing, Haoran, Brain Swenson, Stacia kept the flow of epi both uninterrupted and flawless. I am grateful for their patience and expertise in growing the large number layer structures of the highest quality.

I would like to thank my friends who made good times memorable and challenges short-lived. Many thanks are due to Mishra's, Rodwell's and Bowers's group members of the past and present who collaborated and helped me to give my best every day at every point. I thank Geetak, Jeonghee, Jing, Elaheh, Karin, Matt G, Matt L, Steve, Chris,

Nidhi, Seshadri, Ajay, Sansaptak, Nik, Srabanti, Yi, Man Hoi, Uttam, Vibhor, Vinay, Advait, Avantika, Chirag, Aanchal, Brian R, Silvia, Mahher, Onur, Geza, Ramya, Sathya, Dave Browne, Trey, Xun, Haoran, Erika, Andy, Evan, Vaibhav, Prasanna, Rajeev, Zile, Sumit S, Sumit P, Priyanka, Johaan, Davide, Prateek, Baishakhi, George, Nirav, and Swati. It's an absolute privilege to have spent time with them and to have been treated so well. I am grateful to Val who was always willing and generously guided and helped me in all things administrative and at times personal. Gratitude is also due to Dr. Jeff who shared invaluable insights and strategies that kept me committed to the task.

I would like to thank Prabuddh, Deeksha, Sukanya, Rup and Sumit for proof reading the dissertation.

In every battle, there were four people - my parents, sister and husband who held the fort. The work is a sum of their contributions. I am grateful to my family who never let finances be a deterrent to my education. A sense of perspective was always coming from my parents and kept the focus intact. My sister, Deeksha, has been most generous in helping me refine my writing, ideas and outlook. I have also had untold support from Prabuddh, my husband. He unreservedly collaborated in finding simple approaches to problem solving. The work in many parts reflects his creativity to simplify, my father's ways of finding self-belief and magical spontaneity, my mother's training to plan as well as practice and the unconstrained resourcefulness and playfulness of my sister. A thanks is also due to my parents-in-law. It is my good fortune to have such a family and to have their love and support.

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Abstract

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by

Shalini Lal

The use of epitaxial junctions, especially heterojunctions, like InGaAs/InAlAs, AlGaN/GaN, has yielded transistors switching at high frequency or high voltage. It is however generally found that a high frequency transistor remains deficient in breakdown voltage and vice versa, a limitation of heterojunctions between similar materials by epitaxial methods. Wafer bonding, on the contrary, allows junctions between mismatched materials, and so may be a promising technique to overcome the trade-off between high frequency operation of and the available power from a transistor. This work focuses on the experimental demonstration of a well-behaved wafer-bonded junction and transistor, namely, an InGaAs/InGaN junction and an InGaAs/III-Nitride transistor, respectively. The latter is referred to as a wafer-bonded current aperture vertical transistor, BAVET, comprising a channel in InGaAs and a drift region in InGaN/GaN. In this work, key features of a BAVET are identified, designed, and fabricated. Fundamental to the operation of the transistor is the design of a conductive aperture and an insulating current-blocking layer (CBL). This property in a BAVET results in an on current as high as 600 mA.mm^{-1} and a transconductance of 132 mS.mm^{-1}. Despite the fact that these results mark the first demonstration of transistor operation in a BAVET, other aspects of the on- and off-state performances remain weak. For instance, saturation voltage, on-resistance, turn-on voltage, and output conductance are anomalously high and off-state pinch-off is poor.

Mechanisms pertaining to virtual gate, drain resistance, weak field plating and trap

ionization are found to be the cause of these anomalies. Experiments prove that all anomalies are local to the wafer-bonded interface (WBI). This work determines that passivation of traps at WBI is a solution to these drawbacks in device performance. An in-situ trap passivation process is devised, which uses hydrogen species and the layer structure electrostatics to effect trap activity. This improves all aspects of the BAVET performance, with the saturation voltage, drain resistance, turn-on voltage and output conductance significantly lowered and critical field to trap-ionization made higher.

In addition to designing the BAVET, the dissertation makes progress in understanding the physics of WBI and its relation to functioning of a BAVET. In passivating traps at WBI, a means to improve the wafer-bonded junction and transistor is conceived. The work succeeds in demonstrating a trap-free wafer-bonded InGaAs/InGaN junction, an anomaly-free III-Arsenide/III-Nitride vertical transistor and so reveals a new space of possibilities in the field of wafer-bonded electronics.

Contents

Chapter 1

Introduction

Electronic devices that employ heterojunctions have improved in various applications such as lighting, energy harvesting and high frequency and power electronics. For instance, they have made light emitting diodes, solar cells more efficient and enhanced frequency and breakdown in transistors [1, 2, 3, 4, 5].

A novel heterojunction of InGaAs/Ga(In)N and a vertical transistor design to advancing high frequency power electronics has been proposed in an earlier work [6]. It succeeded in (a) forming the InGaAs/Ga(In)N heterojunction by the method of wafer bonding, (b) providing a basic fabrication technique for a transistor that comprises a waferbonded heterojunction, (c) and experimentally showing a partial transistor behavior, which was a promising first step in the development of wafer-bonded electronics. These developments by Snow et al. served a basis for this dissertation's progress.

Fig. 1.1 shows the timeline of and progress made by this dissertation in advancing wafer-bonded semiconductor transistor technology. The work by Snow et al. was modified in wafer bonding, design and fabrication of the transistor to yield its fully functional DC characteristics (see Fig. 1.1) [6]. At this stage, however, the properties of transistor and the related role of wafer-bonded heterojunction or interface (WBI) are scarcely

understood. The dissertation attempts to extend this knowledge. Different types of electrical measurements on a varied set of devices and experiments are performed for understanding both transistor and WBI performances (see Fig. 1.1). The data is analyzed and statistically correlated to isolate key device physics and phenomena. In this process the dissertation deduces certain fundamental properties pertaining to WBI and transistor and establishes methods to enhance their performance (see Fig. 1.1).

1.1 Motivation Behind Wafer-Bonded Transistors

1.1.1 Transistors by Heteroepitaxy

Research in transistor development has been mainly motivated by the demands of higher operational frequency, as well as voltage in electronic applications. Development in epitaxial methods has enabled formation of transistors comprising heterojunctions like AlInAs/GaInAs, and AlGaN/GaN. The use of a heterojunction has enhanced the performance and design space of transistors. Band engineering in an InP-based heterojunction bipolar transistor (HBT) has been shown to yield enhanced current gain and operational frequency [4]. Whereas in the case of a high electron mobility transistor, a heterojunction induces a channel comprising 2- dimensional electron gas (2DEG) and provides the band offset for gate-modulation of the 2DEG [7] (see Fig. 1.2). The performance benefits are depicted in Fig. 1.3(a), wherein InP and GaN-based heterojunction transistors are able to switch at a higher frequency and breakdown voltage than those comprising Si.

1.1.2 Wafer-Bonding to Enhance Performance of Transistors

The development of transistors in a material system is determined by theoretically derived roadmap of frequency or on-resistance vs. breakdown (see Fig. 1.3) [8], [9].

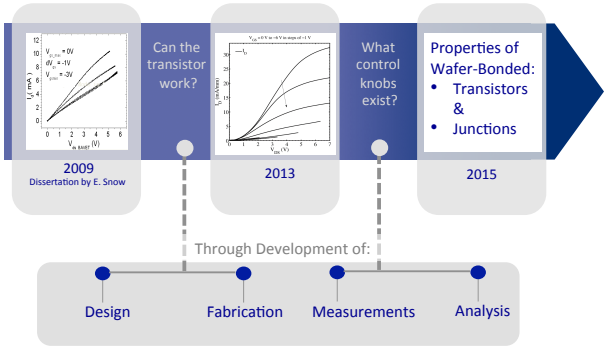


Figure 1.1: A flow chart diagram represents the timeline and stages of this dissertation work. An initial work by Snow et al. yielded a wafer-bonded transistor characteristics shown in the first frame [6]. This dissertation extends on that work and modifies transistor's design and fabrication methods to enhance the DC performance. A fully function transistor behavior is obtained and is shown in the middle frame. Snow et al. to that shown in middle frame. The latter part of this work deals with correlating and analyzing different types of measurements to deducing the mechanisms and electrical properties of wafer-bonded transistor and junctions.

A common attribute that is reflected in such roadmaps is that a gain in operational frequency or reduction in on-resistance is made possible at the expense of a reduction in the highest operable voltage, and vice versa. Thus, the development is stifled by the limits set by the choice device design and material system.

As shown in Fig. 1.3, InP based high electron mobility transistors (HEMTs) [10] and heterojunction bipolar transistors (HBTs) [4] dominate the applications requiring near-terahertz switching operation. On the opposite hand, GaN-based transistors have demonstrated enhanced output power in the sub-terahertz regime [5]. Thus, integrating these two distinct material systems in a transistor is a promising approach to further improving power switching operation at ultra-high frequencies.

The challenge opens up an opportunity of exploration in choosing more than one material system and combining them into one structure for the transistor. In such a transistor, the trade-off arising from material limit placed by a material system on a parameter, such as breakdown voltage in InPbased system, can be avoided in the following manner. If an InP-based transistor incorporates a second material system, such as

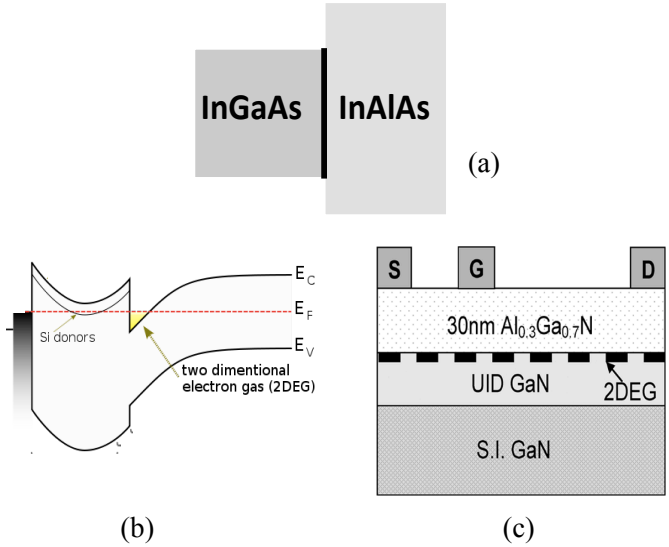
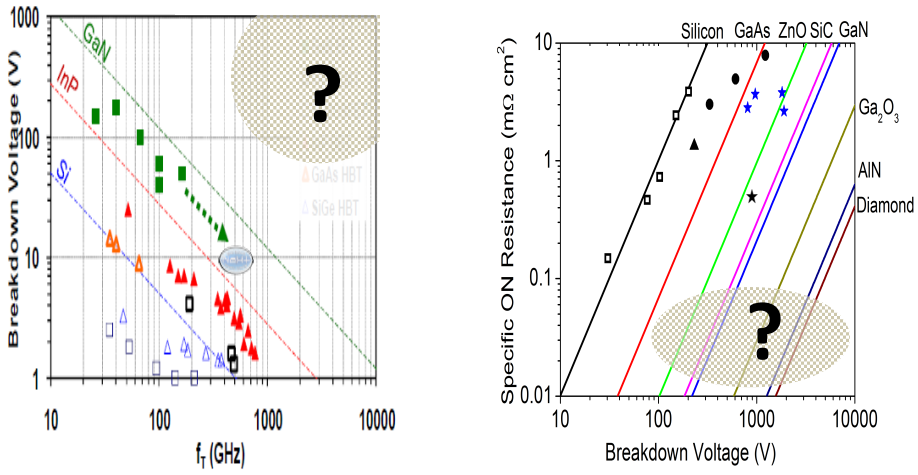


Figure 1.2: An example epitaxial InGaAs/InAlAs heterojunction is shown, wherein InAlAs is a wider bandgap material than InGaAs. (b) An energy band diagram of a doped InAlAs/InGaAs junction is shown to highlight 2DEG formation in InGaAs. A 2DEG channel is a fundamental advantage in a high electron mobility transistor (HEMT). A HEMT's schematic is shown in (c) which is based in III-N material system and comprises an AlGaN/GaN heterojunction.

GaN, which supports higher breakdown limits, then the trade-off can be overcome. An III-Arsenide (III-As)/IIINitride (III-N) transistor is a promising candidate to simultaneously achieve the two figures of merit of frequency or on-resistance and breakdown in a transistor (see Fig. 1.4).

Investigations may then start by forming a heterostructure comprising both III-Arsenide (III-As) and III-Nitride (III-N) material systems. But such formation is difficult to achieve by means of currently available epitaxial methods, as these are limited to materials systems that are close to similar in their crystal properties. An attribute made absent by widely dissimilar crystal structures and lattice parameters between IIIAs and III-N materials. Epitaxy is thus not suited for forming a III-As/III-N transistor structure but is achievable by an enabling technology called wafer bonding [11].



(a) (b)

Figure 1.3: Breakdown voltage vs. (a) current-gain cut-off frequency (f_t) and (b) on resistance trends is shown for different semiconductor technologies [8], [9]. Each technology's development follows a slope that presents a trade-off in between breakdown and f_t or on resistance. The circled region illustrates the untapped performance potential in transistor design. And whether a THz power transistor is achievable by a wafer-bonded transistor based on both IIIAs and III-N material systems is the motivation behind this work.

1.1.3 Wafer-Bonded Transistor - BAVET

A III-As/III-N structure can be fabricated into a transistor. A special case of wafer-bonded transistor arises when a transistor comprises of channel derived from a material system different from the one that contains the drift region.

The purpose is served in a type of wafer-bonded transistors called wafer-bonded current aperture vertical electron transistor (BAVET). A BAVET has its design based on principles of a CAVET [12] with certain exceptions. Like a CAVET, a BAVET also comprises of gate-barrier, channel and a drift region with aperture and CBL (see Fig. 1.5(a)). A part of the device's active region comprises of an interface, named wafer-bonded interface (WBI), which is what makes BAVETs unique from CAVETs (see Fig.1.5(a)). The interface is named such, on account of its formation through the process of wafer

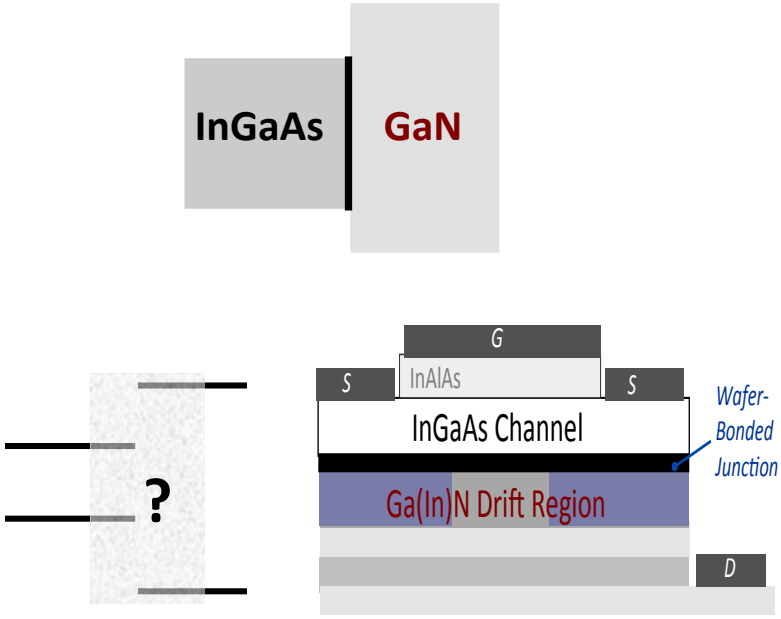


Figure 1.4: The study focuses its investigation on InGaAs/Ga(In)N junctions, the properties of which are less known. Additionally a novel III-As/III-N transistor comprising this junction and its properties are proposed and demonstrated.

bonding.

Introducing InGaAs/InGaN wafer bonding in a CAVET structure helps meet the following two intentions: (a) an InGaAs channel to provide a high mobility or high injection velocity transport of the current-carrying electron, (b) that is collected in a drift region of wider bandgap GaN-based material capable of withstanding high electrostatic fields.

Operation of a BAVET is initiated at the source contact with the injection of electrons into n-doped InGaAs. The electrons transit laterally through InGaAs, which is sandwiched between InAlAs and CBL (see Fig.1.5(b)). InAlAs and CBL layers create a barrier to electron in the direction of both gate and drain respectively. Applying bias voltage to the gate controls the channel conductivity in the LGO regions (denoted by LGO in Fig. **??**(b)). Once the electrons exit the LGO region, the applied drain voltage pulls them towards an n-doped InGaN aperture. Electrons enter InGaN aperture from

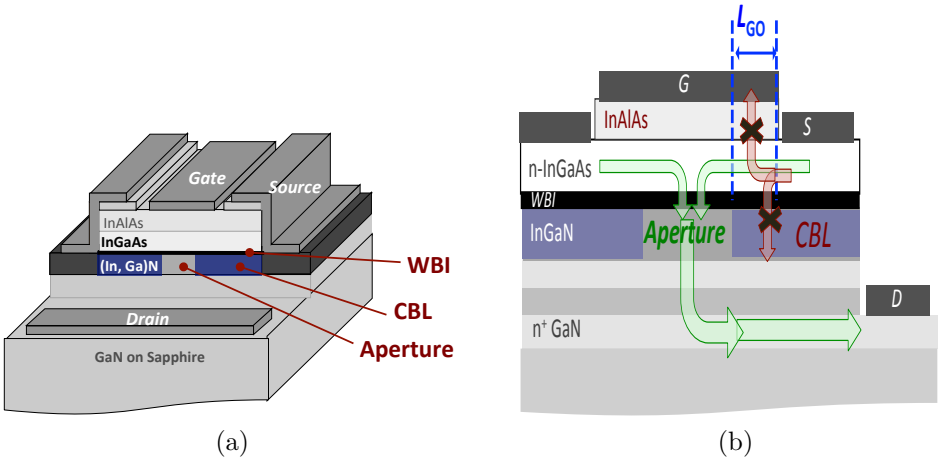


Figure 1.5: (a) A 3-dimensional view of a BAVET is shown. Among its features are an InAlAs layer acts as a gate-barrier to a channel in InGaAs and the stack of InGaN, GaN layers provides for drift region. InGaN layer is ion implanted in selected regions referred to as the current-blocking layer or CBL regions. The region in InGaN that is disposed between the two CBL regions is referred to as the aperture. Aperture and CBL are features that implement the vertical topology of the device. WBI is an additional feature added by the process of wafer bonding. (b) A cross section schematic of a BAVET showing the gate-modulated L_{GO} regions of InGaAs. Gate-modulation happens on account of current blocking in directions towards InAlAs and CBL barriers in L_{GO} regions, which is denoted by crossed-out arrows. A second set of arrows mark the conduction path of electrons from the source contact to the drain-contact, through the L_{GO} regions of the channel, WBI, drift region and terminating at drain electrode.

InGaAs, through the WBI. The transit of electron in the vertical direction is confined to the aperture by the presence of CBL-induced barriers on either sides of the aperture. The electrons transit through the drift region and are collected at the drain-contact. Aperture and CBL together implement the function of transporting only the gate-modulated electrons from the source contact to the drift and so are critical for transistor's saturation and pinch-off.

The operation described herein is similar to CAVET but the role of WBI in that of a BAVET is understood and presented in detail in the course of this work. It finds WBI to be a key feature that determines both operation and performance of a BAVET.

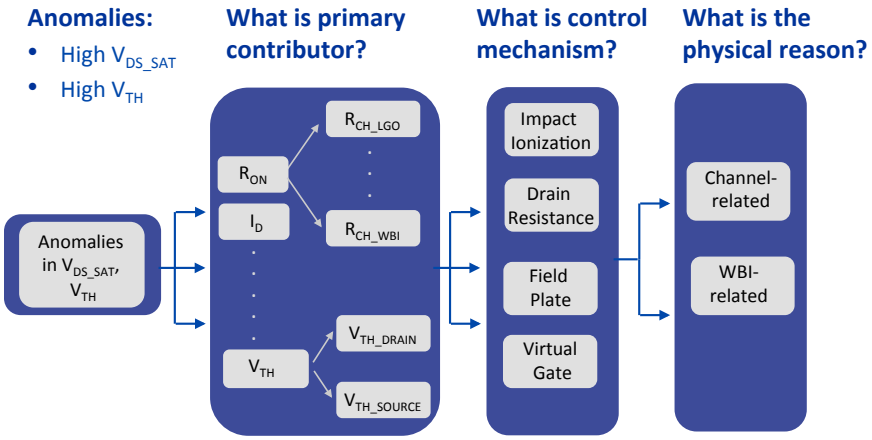


Figure 1.6: The analysis presented in this work follows a process of investigation shown in the form of a flow chart. It uses a process of elimination on different experiments and measurements results. Anomalies in device characteristics like saturation voltage ($V_{\mathrm{DS\_SAT}}$) and threshold voltage (V_{TH}) are identified, they are then isolated into different components and their underlying mechanisms. The end goal of this analysis process is to identify the physical source of anomalies, whether it is the choice of material especially that of a channel or if it's the WBI.

1.2 Scope of Dissertation

One of the intentions of this dissertation is to experimentally realize near ideal behavior in a BAVET and WBI (see Fig. 1.1). Identifying and report the key properties of the two is another goal of this dissertation (see Fig. 1.1).

Chapter 2 and 3 address the first goal of establishing the fabrication process of a BAVET and its design of aperture and CBL regions, respectively. The first DC transistor operation is demonstrated.

Anomalies in BAVET characteristics are identified and the underlying properties are deduced. Methodology to analysis is proposed in Chapter 4 (see Fig. 4.6). Anomalous nature of saturation and threshold voltages is explained and related theory is formulated using device physics in Chapters 4 to 6. Anomalies are proved to arise on account of parasitic effects, for instance, virtual gate effect, and low critical field to impact-ionization of WBI.

The study leads to identification of trap-affected WBI as the anomaly-causing feature of a BAVET in Chapter 7 and reports a method that modifies trap behavior of WBI and consequently BAVET's characteristics. Experiment results in a nearly trap-free WBI and anomaly-free BAVET characteristics, which are the two major performance enhancements achieved by this work.

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Chapter 2

Fabrication

BAVETs or wafer-bonded devices in this dissertation are fabricated in a three-phased process. The first of which involves growth of the required epitaxial structures. The structures are wafer-bonded to form another stacked structure in the second phase. And in the final and third step the structure is processed to result in an electronic device.

2.1 Phase 1: Designing Epi-Layer Structures

For a BAVET, two structures, namely III-Arsenide (III-As) and III-Nitride (III-N) are grown by epitaxial techniques.

2.1.1 III-As Structure

The III-As epi-layer structure is grown by molecular beam epitaxy on a 4 inch InP substrate, at IQE Inc. and IntelliEpi (see Figure 2.1a). All the InGa(Al)As layers are grown lattice matched to InP. Two etch-stop layers of 100 nm InGaAs and 20 nm InP are grown consecutively on the InP substrate. This is followed by the growth of a 10 nm InGaAs ($[\mathrm{Si}] = 3 \times 10^{18}$ cm^{-3}) cap layer and a 50 nm InAlAs layer which is doped p-type

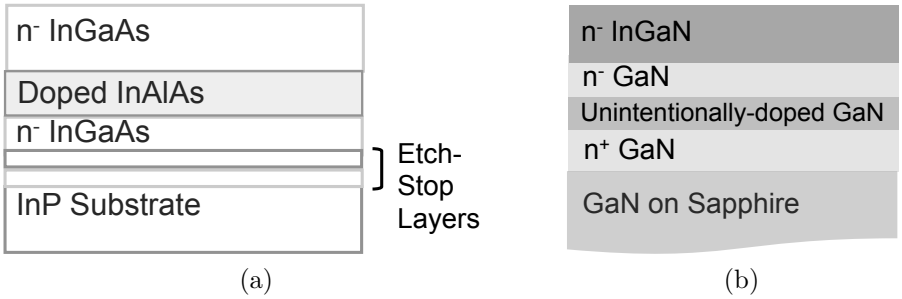


Figure 2.1: Cross section schematics of III-As and III-N layer structures.

([Be] = 5×10^{18} cm^{-3}) . Finally, a 150 nm InGaAs channel (with an electron charge density of 3×10^{12} cm^{-2}) forms the top layer of the III-As template. InGaAs channel is the wafer bonding layer of the III-As structure.

2.1.2 III-N Structure

The III-N structure is grown Ga-polar on a sapphire substrate (see Figure 2.1b). It comprises a Fe-doped semi-insulating GaN on sapphire, an n+ GaN layer on semi-insulating GaN, an unintentionally-doped (UID) GaN on n+ GaN, an n- GaN layer on UID GaN, and an n- InGaN layer on n- GaN.

All III-N templates in this work are grown with a Ga-polar orientation on a 2 inch sapphire substrate by metal-organic chemical vapor deposition (MOCVD). The epitaxial growth starts with a thick Fe-doped semi-insulating GaN, followed by a 1 μm thick n-type GaN ([Si] = 5×10^{18} cm^{-3}) for the drain contacts. On top of the drain-contact layer, two more GaN layers are grown consecutively (see Figure 2.1b). The first layer is unintentionally doped (UID) 0.8 μm thick, on top of which, a 0.3 μm thick second layer is grown. Finally, a 50 to 125 nm of $In_{0.1}Ga_{0.9}N$ or InGaN layer is grown at a temperature of 890°C on top of the GaN template. The required n-doping in the top InGaN and GaN layers are determined based on the desired aperture conductivity. The

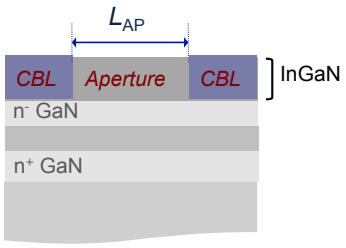


Figure 2.2: A schematic showing the aperture and CBL regions formed by ion-implantation of InGaN layer. L_{AP} denotes the length of the aperture.

sandwiched InGaN layer reduces the effective conduction band barrier for the electrons traveling from InGaAs to GaN [1] thereby improving the vertical conduction of electrons.

An asymmetric off-axis reciprocal space map measurement on the III-N template indicates that the InGaN layer is fully strained to the GaN buffer. This strain causes a net negative piezoelectric component of the polarization charge exists at a Ga-polar InGaN-GaN interface, which in turn induces a conduction band barrier. Eliminating this barrier is required for high current conduction and it can be achieved by either δ-n+ doping the InGaN-GaN interface [2] or by changing the III-N polarity to N-polar growth mode [3]. This dissertation focusses on the former approach of doping the interface.

2.1.3 Ion implanting InGaN to form current-blocking region

The InGaN layer, which is the wafer bonding layer of the III-N structure, is conductive in some regions while insulating in the remaining. The insulating region of the InGaN is referred to as the current-blocking layer region (or CBL), and surrounds a conductive region on either side (see Figure 2.2). These conductive openings in a mainly insulating region are referred to as aperture (denoted by L_{AP} in Figure 2.2. Selective ion implantation is performed to create CBL regions in n- InGaN.

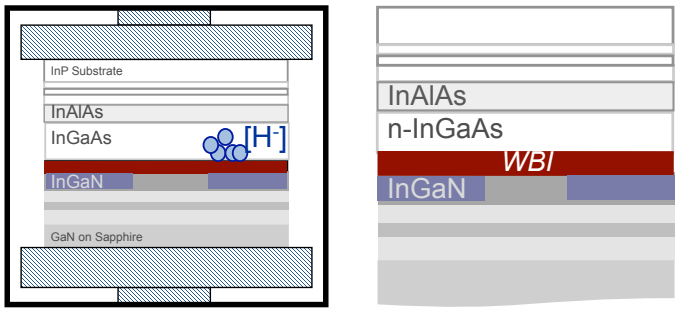
The III-N template is first patterned with a SiO_2/Ti/Ni mask and then selectively implanted with [Al^+] ions (dose =10^{15} cm^{-2}) at an implantation angle of 7 degrees. After

implantation, the mask is removed using acid-based wet etching process. An anneal is then performed on the III-N template using an MOCVD reactor. Mobile point defects incurred by the crystal from the implantation process are healed in the anneal step. It does so while retaining the insulating properties of the implant. The energy of the implant required to obtain a CBL with a strong insulating behavior, depends on the desired thickness and the background n-doping of the aperture/CBL containing layer. The insulating properties of the CBL are characterized by varying the implant energy while keeping the implantation species, dose and angle constant. The III-N template with a CBL and aperture defined in the InGaN layer is shown in Figure 2.2.

2.2 Phase 2: Wafer Bonding and Trap Passivation

2.2.1 Wafer-bonding III-As and III-N structures

Wafer-bonding is a crucial step in the fabrication of a BAVET. In a BAVET, the implanted III-N template is wafer-bonded to the as-grown III-As epi-layer structure. Absence of particles and smooth surface morphology of the interacting surfaces, are the two essential prerequisites in maximizing the strength and extent of the wafer-bonded interface. To make the surfaces devoid of particles, a solvent-based rigorous cleaning procedure is performed on the two templates. An ultra smooth surface morphology of the III-As template can be achieved from the matured growth technology of the III-(P)As material system. However, the surface morphology of the III-N template used in a BAVET exhibits macroscopic undulations which currently limits wafer-bonding yield to approximately 2 cm $\times$ 2 cm sized samples [4]. These undulations are the result of the thickness non-uniformities characteristic to the MOCVD reactor design used in the III-N growth on a 2 inch sapphire substrate. Prior to wafer-bonding, the surfaces of the two



(a) (b)

Figure 2.3: (a) A cartoon of wafer-bonding process is shown. The stack of two structures is placed between two tool plates (denoted by shaded regions disposed on top and bottom of the semiconductor stack) of a wafer bonding system. Pressure is applied to the tool plates such that the structures of III-As and III-N are pressed against each other. During wafer-bonding a passivation process is also initiated. It herein requires hydrogen ions as passivation species. (b) The resultant structure of the wafer bonding process is the wafer-bonded structure comprising WBI and both the semiconductor structures.

templates undergo repeated solvent cleans, native oxide removal using buffered hydroflouric acid (BHF) etch and an oxygen-based plasma activation. The plasma activation assists in achieving wafer-fusion at lower temperatures by forming a hydrophilic surface on the interacting III-N and III-As templates [5]. The III-As epi-layer structure is then flipped and placed on top of the III-N template. The structure is then moved into the Suss Microtec SB6e bonder and wafer-bonded by pressing the interacting surfaces against each other for three hours at an applied pressure of 5 MPa and at a temperature of 400°C. The resulting wafer-bonded layer structure is shown in Figure 2.3a. Wafer-bonding yields a structure which comprises a WBI between n- InGaAs and n- InGaN layers forming a WBI (see Figure 2.3b).

2.2.2 In-situ Passivation of Traps at Bonding Interface

A method to passivate traps of WBI during wafer-bonding is developed in this work. The method will be presented in detail in another study but is briefly discussed herein.

InGaAs channel plays the role of a passivation-releasing layer containing hydrogen as the passivation species, while InAlAs is a passivation-blocking layer. The electrostatics of passivation-releasing and blocking layer migrate hydrogen ions to WBI. Interaction of these ions with traps, if any,at WBI leads to their passivation during the wafer bonding process.

2.3 Phase 3: Device Processing

The InP substrate and etch-stop layers are then removed by acid based wet etch process. Finally, an n-InGaAs/InAlAs/n-InGaAs structure fused to a (In)GaN layer structure is obtained (see Figure 2.4) and is then processed into a BAVET using conventional fabrication techniques.

2.3.1 Substrate Removal

The constituent III-As structure also contains etch stop layers (see Figure 2.1a). These etch stop layers enable the removal the unwanted substrate/layers from the wafer-bonded structure. After substrate removal, resultant device structure comprises semi-insulating GaN on sapphire, n+ GaN on semi-insulating GaN, UID GaN on n+ GaN, n- GaN layer on UID GaN, CBL-aperture-containing n- InGaN on n- GaN, n- InGaAs on the CBL-aperture-containing n- InGaN, and InAlAs on n- InGaAs. The InAlAs is the gate barrier layer, n- InGaAs is the channel, and drift region comprises the region between the InGaN aperture and drain-layer of n+ GaN (see Figure 2.4). The structure is referred to as the device structure.

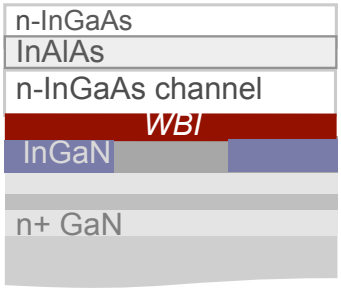


Figure 2.4: Cross section of III-As/III-N structure after substrate removal, wherein the III-As substrate and etch-stop layers are removed after wafer-bonding.

2.3.2 Electrode and Mesa Formation

Source-contact is made to the n- InGaAs channel in the region which overlaps with the CBL. The InAlAs layer is etched in this region of the source-contact, and source metals (AuGe/Ni/Au/Ni) are deposited (see Figure 2.5). Two source-contacts are deposited on the channel in the regions on either side of the InAlAs layer. Another etch is performed for device isolation (see Figure 2.5a). The isolation-etch removes the III-As, and III-N

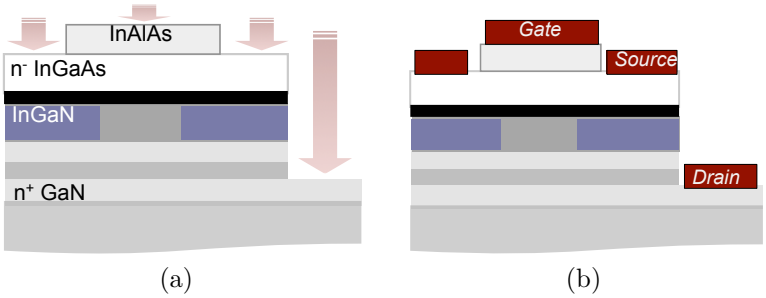


Figure 2.5: (a) Device schematic is shown to highlight different etch processes that are employed. Formation of source contacts to n-InGaAs channel requires etching InGaAs cap layer and InAlAs in in the CBL regions. A block arrow is used to point to the region that is etched. Isolation etch is performed in the device, and a stack of layers (InAlAs/InGaAs/InGaN/ n- GaN/UID-GaN) are etched till n+ GaN is reached. This isolation etch also reveals the region to deposit the drain contact. For the gate process, the InGaAs cap layer is etched. (b) Gate, source and drain metallization to the device schematic are illustrated. Metal (AuGe/Ni/Au/Ni) is deposited for source contact. Drain contact (Al/Au) is deposited on the n+ GaN layer. Gate metal stack of Ti/Pt/Au/Ni is deposited on InAlAs.

layers until the n+ GaN layer is reached. The drain contact (Al/Au) is deposited on n+ GaN (see Figure 2.5a). The gate contact (Ti/Pt/Au/Ni) is deposited on InAlAs in the region that is disposed in between the two source-contacts, and that overlaps with the InGaAs in both CBL and aperture regions (see Figure 2.5b).

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Chapter 3

Design Features

3.1 Introduction to Design of a BAVET

Can a unipolar wafer-bonded transistor, BAVET, function as a transistor? If it works as a transistor then does it suffer from any abnormalities in its performance? What are the key features that not only make the transistor work but also make it work without anomalies. These are some of the questions answered in this work.

In designing the aperture and current blocking layer (CBL) of a BAVET, one may find the answer to the first question. The abnormal nature in a BAVET if originates at the wafer-bonded interface (WBI), then designing for a well behaved WBI may hold the key to a well behaved performance in a BAVET. So the second question may be answered. In answering these two questions, the study also reveals information on the third unknown. Designing aperture, CBL and WBI, may be tightly coupled to dramatic improvements in the performance of a BAVET and therefore they may well be the features that yield a BAVET. The study presents three experiments, each pertaining to a feature.

3.1.1 Introduction to Design of Aperture and CBL

A vertical transistor of the form of a CAVET functions as a transistor on account of the presence of CBL and aperture [1]. A channel carries the current laterally and an aperture does it vertically. To set a current path such as this, it is necessary that a current-blocking layer (CBL) be present in regions below the channel and around the vertically conducting aperture (see Fig. 3.1). The conductive aperture and blocking CBL end up becoming different regions of a semiconductor layer. The challenge lies in obtaining two regions that are part of the same layer but hold contrasting properties in current conduction. Aperture must flow as much current that is injected from the channel. A current conducting CBL, on the contrary, unfavorably contributes to leakage in a CAVET. In this work, we are tasked with finding aperture and CBL design for a BAVET, which comprises of a channel in InGaAs; and aperture and CBL in an InGaN layer.

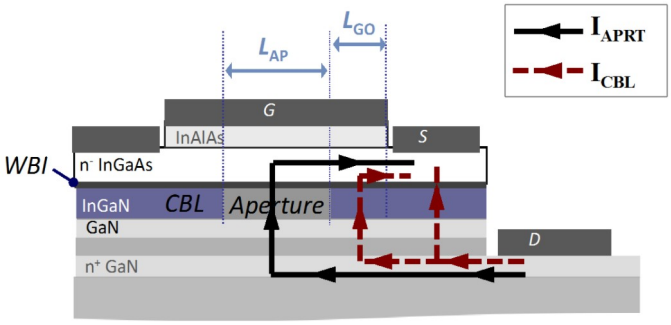


Figure 3.1: A BAVET schematic shows the aperture, CBL and WBI. InGaN layer contains the aperture and CBL. InGaAs-InGaN is WBI. Gate barrier is comprised in InAlAs. Currents flowing through the aperture and CBL are shown as solid and dashed lines, respectively. G, S, D denote the gate, source and drain electrodes of a BAVET. Gate overlaps with channel-CBL in L_{GO} region and with the aperture in L_{AP}.

The investigation, starts with explaining the use of n-doping and ion-implantation to design aperture and CBL, respectively. The quality of aperture and CBL can be measured in on current and leakage of a BAVET. Two experiments are conducted: aper-

ture and CBL experiments. Variation to aperture current by n-doping is studied in the aperture experiment. CBL experiment, on the other hand, tests CBLs with different ion-implantation energies for low leakage. Apertures with low and high n-doping concentrations are compared. Highest aperture conductivity, or current, is obtained if the doping is high and δ-doped at an interface between the InGaN and GaN layers. A relationship between polarization of III-Nitride region of the BAVET and its aperture conductivity is illustrated.

CBLs are fabricated and tested for a range of ion-implantation energies between 20 and 63 KeV. Only 53 and 63 KeV CBLs show lowest leakage. An explanation of this outcome is posited. Due to the change in the nature of point defects, in ion implanting at one or the other energy, differences are observed in leakage characteristics of different CBLs. High energy CBL and δ-doped aperture are found to be the two necessary conditions towards low turn-on voltage, low leakage, high on current and, most importantly, a transistor operation in BAVETs.

3.1.2 Introduction to Design of WBI

A certain aperture and CBL design obtains us a transistor action in a BAVET. The performance of which is further improved in another experiment, referred to as the WBI experiment, wherein the doping in the gate barrier layer, InAlAs, is modified. Gate-barrier doping dramatically impacts the three device parameters, namely, turn-on voltage ($V_{\mathrm{DS\_ON}}$), saturation voltage ($V_{\mathrm{DS\_SAT}}$), and output conductance (G_{OUT}). The phenomenon is unrelated to change in channel conductivity but arises from a change in behavior of InGaAs-InGaN WBI. The experiment brings out an interesting fact that a doping in a layer, which is the gate barrier that is remote to WBI, has a dramatic influence on the electronic properties of the latter. This improvement in WBI behavior eliminates

anomalies in a BAVET and so makes it well behaved in multiple device parameters.

The three experiments on aperture, CBL, and WBI are interrelated. For instance, the most conductive aperture from the aperture experiment is chosen for the BAVETs studied in the CBL and WBI experiments. Therefore, in the description of each experiment is contained not only the design changes, but also its results and discussion.

3.2 Methods to Design and Characterize Aperture and CBL

3.2.1 Aperture Conductivity by n-Doping

For InGaAs/InGaN BAVETs discussed herein, aperture and CBL reside in the InGaN layer. n-doping the InGaN produces the conductive nature in apertures and on changing the dopant concentration, the aperture conductivity is varied. The decisions on doping concentration and what region of the layer is to be doped rely on magnitude and location of a barrier, if it exists, that inhibits electron flow. A barrier may arise as a consequence of the polar nature of the III-Nitride, especially that of the InGaN-GaN interface (see Fig. 3.1).

The two ends, one that is next to InGaAs and the other to GaN, are the Gallium- and Nitrogen-faces of InGaN layer, respectively. These faces are bound to oppositely ionized polarization charges. These charges, if uncompensated, produce electrostatic field that either aids or works against the one due to a doped junction [2]. Therefore, polarization at the interfaces needs to be considered in choosing the concentration and position of n-doping for an aperture.

Once InGaN is doped for aperture, CBL regions may be formed. As recalled from the earlier section, CBL is, by name and principal, a region whose conductivity should

be as low as possible. How to form a CBL is the subject of next section.

3.2.2 Ion-Implantation for CBL

Countering n-type conductivity by ion implantation is an effective method to create CBL [1]. For a given target layer, the strength of current blocking may depend on a number of factors ranging from conditions like type of ion-implantation ion dose, and energy [1], [3]. The conditions that were previously deduced for GaN in CAVETs act as a sound basis to the study of finding those suited for InGaN layer of BAVETs [4].

The study follows ref. [4] in the choice of the type of ion and the ion-implantation dose, namely aluminum ions [Al^+] and 10^{15} cm^{-2}, respectively. The energy of ion-implantation is adjusted based on the difference in the In composition, the thickness and n-doping of an InGaN layer of a BAVET, and that of a GaN layer in a CAVET. This study characterizes a range of energies as InGaN CBL.

3.2.3 Device Parameters Impacted by Aperture and CBL

It is necessary to center the investigation on those parameters of a BAVET that are directly impacted by the properties of aperture and CBL. Conversely, the quality of the two can be evaluated by the value exhibited for certain parameters of transistor.

Aperture Conductivity and On-Current

The current density available from the device depends on how conductive is the aperture. An explanation of the connection follows. Fig. 3.1 illustrates that the current, I_{APRT}, on exiting the channel is carried in the aperture. Under on state conditions, the InGaAs channel is not fully depleted, and so is not current limiting. But I_{APRT} may be limited in the aperture region if there is a barrier or resistance. Therefore, in having a

conductive aperture, a BAVET is able to operate at high on state currents. In a latter section of the study, aperture with different conductivity will be compared by the I_{APRT} measured for a given drain voltage.

CBL Current as a Leakage

With regards to CBL, transistor functionality is compromised if CBL is leaky. Let us briefly discuss how this happens. CBL is principally the back-barrier for channel with a function of blocking leakage currents. A low barrier has an undesired outcome of electrons transiting unhindered from source-electrode to channel, and into the drain electrode, through CBL. Fig. 3.1 shows leakage currents, I_{CBL}, in L_{GO} and access regions of the device. I_{CBL} is a parasitic current flowing in parallel to I_{APRT} and determines gate-control on the channel.

Gate Control in a Transistor

Gate control in a transistor refers to a mechanism by which an applied gate voltage regulates the channel depletion width and thus, its conductivity [5]. Two key functionalities of a transistor depend on the gate-control. Pinch off of the channel at its drain edge causes the current saturation and that at the source edge aids in switching off the device.

3.2.4 CBL Leakage and Gate Control in a BAVET

I_{CBL} impacts a BAVET in its gate-control. A leaky CBL unfavorably gets rid of the two functionalities in a BAVET. It cannot pinch-off in either case, for the electrons from the source may escape through the back-barrier in both the L_{GO} and access regions (see Fig. 3.1). In measuring source-drain leakage through CBL and/or transconductance (g_m)

in a BAVET, the blocking attribute of a CBL is tested.

3.3 Structure and Layout of Bavet

3.3.1 III-N Layer Structure

The InGaN and adjacent GaN are the two layers that are modified in the aperture and CBL experiments. The remaining III-Nitride (III-N) and the III-Arsenide (III-As) layers are similar to those described in an earlier study [6].

InGaN layer is grown as thick as 50 nm, and can be doped n-type. The layer can be considered as one wide aperture; L_{AP} extends from one edge of the wafer to another. This wide aperture is modified into many narrow ones by selectively ion-implanting the InGaN layer. Ion implanting InGaN in some regions while protecting it in other parts by a metal mask achieves the selectivity. Regions underneath the mask are narrow apertures, and those without it become CBL. The mask is removed prior to wafer bonding. BAVETs are fabricated on wafer-bonded III-N/III-As stack, with III-N comprising aperture and CBL [6].

3.3.2 What L_{AP} to choose?

One can either choose BAVET or diode structures for the measurement of I_{APRT} and I_{CBL}.

I_{APRT} and I_{CBL} are measured in BAVETs that differ in their L_{AP} and are biased in the manner shown in Fig. 3.2. I_{D}-V_{DS} traces are measured while the gate-electrode is kept open. I_{APRT} becomes the current conducted between the source and drain electrodes of a BAVET, which has an L_{AP} that is chosen in a range of 3 to 15 μm (see Fig. 3.2(a)). Source-drain current if measured for $L_{\mathrm{AP}} = 0$ μm represents the current permitted by

a CBL, or I_{CBL} (see Fig. 3.2(b)). I_{APRT} and I_{CBL} can, additionally, be characterized on two-terminal diode structures comprising aperture lengths greater than and equal to zero, respectively.

3.4 Experiments, Results and Discussion

The changes in I_{APRT} and I_{CBL} of BAVETs effectively track changes in the conduction properties for different aperture and CBL designs. Those that exhibit the highest I_{APRT} and the lowest I_{CBL}, become the preferred choice for aperture and CBL.

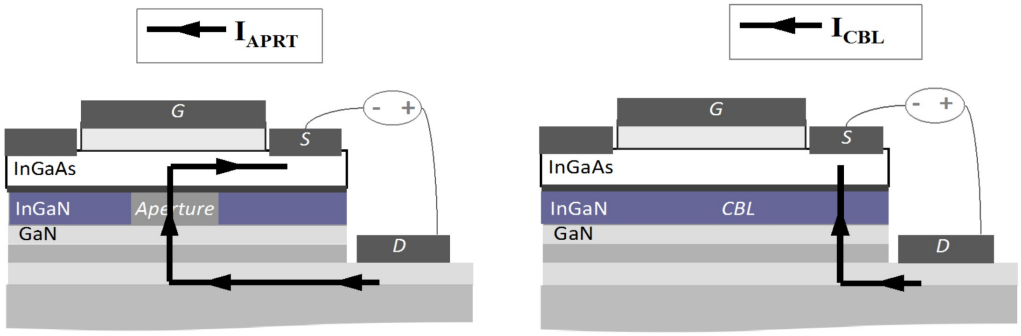


Figure 3.2: Two types of BAVET structures are shown with (a) a non-zero, and (b) a zero LAP. For each device, both source electrodes are grounded while the drain electrode is positively biased. The current paths are shown for one of the source electrodes. BAVETs in (a) and (b) yield I_{APRT} and I_{CBL}, respectively. I_{APRT} is the desired current while I_{CBL} is a leakage in BAVET.

3.4.1 Aperture Experiment

Experiment: Different n-doping concentrations for InGaN and GaN layers

The experiment varies the doping in the bulk of InGaN, GaN layers and their interface. Three doping schemes are proposed. In two, the layers are uniformly doped over their

respective thicknesses. In one such case, referred to as low-doped scheme, InGaN is n-doped at 8×10^{17} cm^{-3} and GaN at 3×10^{17} cm^{-3} (see Fig. 3.3(a)). These concentrations are increased by an order of magnitude for the second doping scheme named as high-doped (see Fig. 3.3(b)).

The layers can be selectively doped to comprise of both high as well as low-doped regions. This is achieved in a third type of doping scheme in which the InGaN-GaN interface is δ-n-doped as the bulk of the InGaN and GaN layers are maintained at low n-doping (see Fig. 3.3(c)). Such a structure is hereinafter named δ-doped.

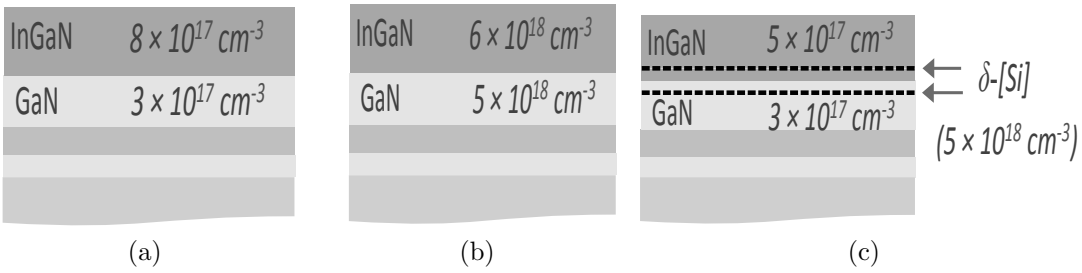


Figure 3.3: Three III-N structures for the aperture experiment are shown. (a) Low doped, (b) high doped and (c) δ-doped structure. Each structure differs in their doping of InGaN and GaN layers.

The three structures for the aperture experiment can analogously be described by the statement that a low-doped structure differs from high and δ-doped in the doping of the InGaN-GaN interface. These three structures are processed to yield BAVETs, referred to as low, high, and delta doped BAVETs. These are characterized by I_{D}-V_{DS} measurements.

3.5 Results: I_{APRT} vs. Doping

On varying the doping from low to high, or δ-doping, there is a marked difference in I_{D}-V_{DS}, which is in contrast to that between high and δ-doped devices (see Fig. 3.4).

For an applied voltage of 4 V, I_{APRT} for δ-doped or high-doped aperture exceeds the low-doped aperture by 5 orders of magnitude. Conversely, the turn-on voltage is lowest for δ- and high-doped apertures. These two designs are so well suited for aperture.

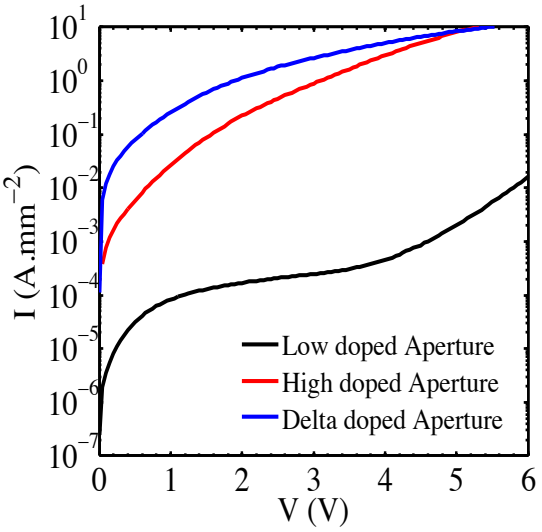


Figure 3.4: The I_D-V_{DS} or I_{APRT}-V_{DS} measurements are shown for different types of aperture. I_{APRT} is scaled by aperture's area. Low doped structure yields lowest I_{APRT}. The apertures have a width of 75 μm. LAP is 10 μm for low and high doped; and 4 um for δ-doped aperture.

3.6 Discussion: InGaN-GaN interface and its Polarization

From an earlier section one can recall that in low-doped structure interface is low doped while in the other two it is doped high. The difference in I_{APRT} for different doping is a result of the difference in the doping of InGaN-GaN interface. We proceed to explain the mechanism by this relation is brought about.

Polarization effects at the interface may need to be considered. For Ga-polar InGaN-GaN homojunctions, piezolelectric polarization causes a net negative charge at the interface [2]. Reciprocal space map measurements for the III-N structure shows that the

InGaN layer is fully strained to GaN layer. The result of such strain is piezoelectric polarization and a net negative charge at InGaN-GaN interface. Negatively ionized charges, if uncompensated, deplete n-doped layers on either side of interface. Depletion electrostatics creates a barrier in the conduction band. It is this barrier, referred to as Ψ_{bi}, that appears in a low-doped aperture, and unfavorably blocks electrons, and so limits current, or I_{APRT} (see Fig. 3.5(a)). High voltage bias is needed to overcome Ψ_{bi} and therefore, the high turn-on voltage.

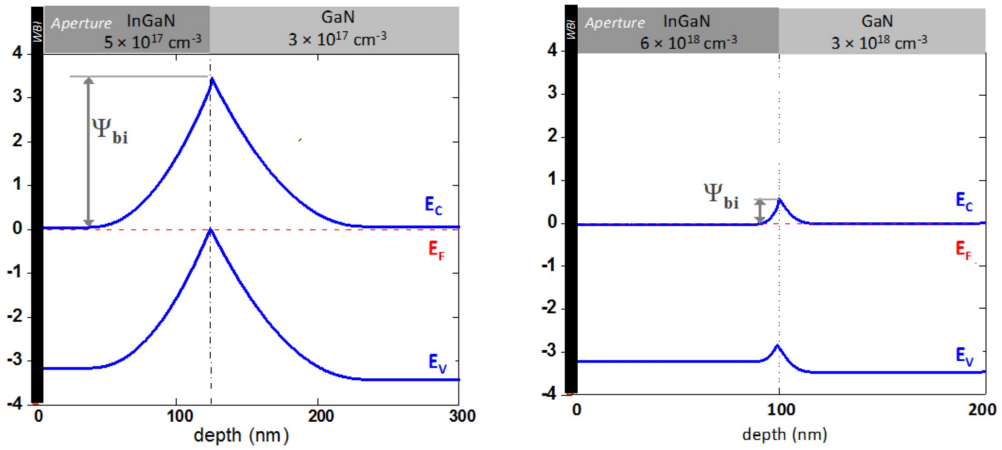


Figure 3.5: The layer structure and corresponding energy band diagrams for (a) low and (b) high doped apertures. These are equilibrium band diagrams that are simulated in Bandeng [7]. E_C, E_F, E_V denote conduction band, Fermi-level and valence band, respectively. Ψ_{bi} is the built-in barrier at the InGaN-GaN interface. Simulation shows higher Ψ_{bi} for low doped than high-doped structure.

Doping the interface high, however, compensates the polarization charges through dopants that are positively ionized. The net interfacial charge is modified such that the higher n-doping, the lower Ψ_{bi} (see Fig. 3.5(b)). In the aperture experiment, doping the aperture high, especially at the interface, either by uniformly or δ-high doping, one succeeds in obtaining higher I_{APRT}, and lower turn-on voltage. In understanding the doping dependence of I_{APRT}, the role of polarization on aperture conductivity is hence

determined.

The aperture experiment yielded conductive apertures, however, the design for a blocking CBL is yet to be found. For this purpose, we conduct a CBL experiment.

3.6.1 CBL Experiment

CBLs are, firstly, designed for different ion-implantation energies and then tested for I_{CBL}.

How to choose the ion-implant energies?

In choosing the ion-implantation energy, one has to meet an initial condition that the damage from ion-implantation should be contained within the thickness of target layer. It is well known that the peak position and the width of the ion-implantation profile, called range and straggle, respectively, increase with the energy of ions [8]. In other words, the position of the CBL changes such that it shifts deeper into the stack as the ion-implantation energy increases.

How to fabricate CBLs of low and high ion-implant energies?

Designing CBLs with different energies in a manner that the CBL is contained within a fixed thickness of a target layer is thus a challenge. We address this challenge in two ways. One way is to implant directly into the target layer at energies low enough to keep the damage well within the layer (see Fig. 3.6(a)). In implant at higher energies, a modified layer stack can be chosen (see Fig. 3.6(b)). In the modified stack, the target layer is implanted through another layer, called a sacrificial layer. This layer is deposited prior to ion-implantation. The sacrificial layer is etched away post ion-implantation, and what is obtained is a high energy CBL in the intended target layer (see Fig. 3.6(b)).

A larger number of CBLs can be designed this way, as wider range of energies is made accessible.

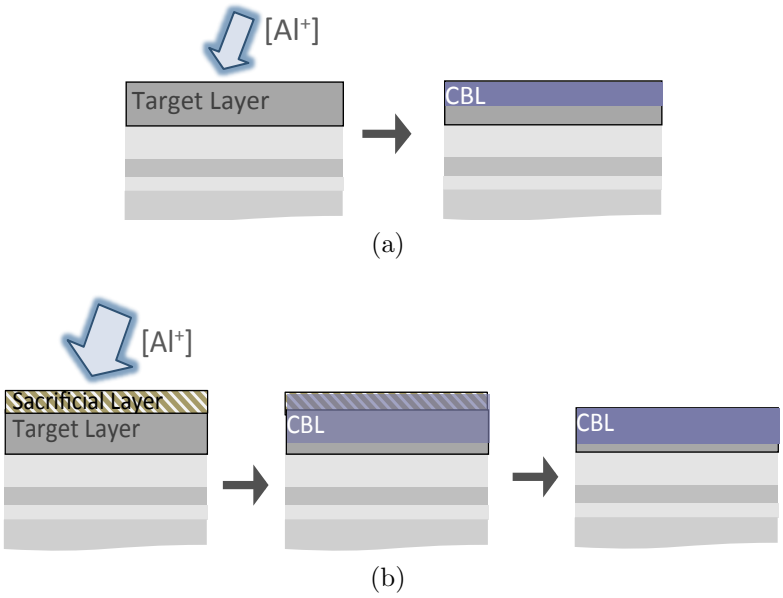


Figure 3.6: Ion-implantation layer stack and process are shown for (a) low and (b) high energy CBLs. The two differ in their layer stack by a sacrificial layer, which is needed for high energy CBL. For (a) the process only comprises of ion-implantation step. The ion-implantation step of (b), however, is preceded and followed by deposition and removal of sacrificial layer, respectively. Herein, BAVETs comprise a target layer, which is InGaN, sacrificial layer of Si_xN_y. CBL of low energy depicts that formed at ion-implantation energy 20 KeV, while those that are high energy employ 43, 53 and 63 KeV.

Experiment: Different Energies for InGaN CBL in BAVETs

For the case of ion implanting InGaN without the use of sacrificial layer, SRIM simulation estimates the energy to be 20 KeV [9]. It is the lowest energy used in this study. Any further increasing in energy increases the ion range and so the CBL unfavorably moves from InGaN to the GaN layer.

Depositing a sacrificial layer of Si_xN_y on the top-surface of InGaN layer circumvents the issue. By SRIM simulation, it is found that a 50 nm thick Si_xN_y works well in

keeping the ion-range within the InGaN layer. And this holds true for a range of energies between 40 to 60 KeV. Any further increase in energy may require an increase in thickness of Si_xN_y.

Four III-N structures are grown, wherein the InGaN and GaN layers are either doped high or δ-n-type. These doping conditions were deduced by the aperture experiment discussed earlier. One among these structures is ion-implanted at 20 keV using a process similar to that described in Fig. 3.6(a). In the other three, Si_xN_y is used for the sacrificial layer. For the ion-implantation energy, the three structures are exposed to 43, 53, and 63 KeV (see Fig. 3.6(b)). Following ion-implantation, Si_xN_y is removed by a wet etch [1].

Confining ion-implantation profile to InGaN meets only one of the critical conditions in the design of a CBL. There is yet another condition that needs to be met. Do these CBL qualify as layer that blocks I_{CBL}? To this end, the four ion-implanted structures are fabricated into BAVETs and/or diodes; and characterized for I_{CBL}.

Results: I_{CBL} vs. Ion-implantation energy

I_{CBL} for the four ion-implantation energies is shown in Fig. 3.7. Lowest I_{CBL} is obtained in those, which have their InGaN layers ion-implanted at 53 and 63 KeV. A significant reduction in I_{CBL} is evident when comparing the I_{CBL} of 43 and 63 KeV. The two differ by six orders of magnitude. The ion-implantation energies to convert an InGaN layer to a current-blocking CBL are hence found to be either 53 or 63 KeV.

The difference of I_{CBL} in 20 and 43 KeV is yet unexplained and needs further investigation. However, we herein attempt on answering the question of why I_{CBL} is such a strong function of ion-implant energy, especially when it is changed from 43 to either 53 or 63 KeV.

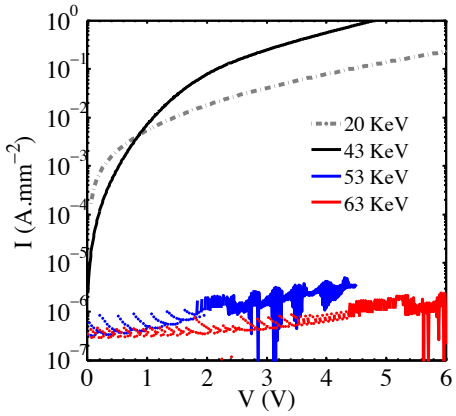


Figure 3.7: I_D-V_{DS} or I_{CBL}-V_{DS} measurements are shown for BAVETs differeing in ion-implantation energy. I_{CBL} is scaled by area of the source electrode. It has a width of 75 μm and a length is 15 μm. 53 and 63 KeV CBLs flow the lowest ICBL.

Discussion: Mechanism by which current-blocking depends on ion-implant energy

A hypothesis is presented for the mechanism behind the current-blocking nature of an ion-implanted region or CBL. In an n-doped InGaN layer, before it is ion-implanted, the Fermi-level is close to conduction band. Ion-implantation creates point defects in the n-doped layer, and so introduces energy levels in the band gap of InGaN. These defect levels can move the Fermi-level closer to the valence band if the following two properties are met. Point defects must be, firstly, not fully compensated by the n-dopants and secondly, associated with energy levels in band gap that are closer to the valence band.

The blocking nature of the ion-implanted layer can then arise from the difference in the Fermi-levels of CBL, which is near valence band, and InGaAs channel. A built in barrier is introduced similar to that in an n-p junction [5]. It is this barrier that brings about the blocking capability in a CBL.

How does the barrier change with ion-implantation energy? The answer to this question can be related to whether the ion-implantation energy changes the distribution of ion-implantation profile or, whether it modifies the nature of point defects.

SIMS on the three ion-implanted structures shows that the implant profile is uniform in InGaN and the ion-range and straggle differ narrowly from one implant energy to another (see Fig. 3.8). But the similarity in their profiles does not translate to similar blocking properties, especially the leakage current is orders of magnitude greater in 43 KeV CBL than that in 53 and 63 KeV CBLs. It is suggested that a uniformly distributed ion-implant profile in the InGaN does not alone make an effective CBL.

It is then stated that dependence of ion-implant energy and I_{CBL} is due to the former changing the nature of the point defects. The change can be explained by an aforementioned hypothesis: point defects, if uncompensated by n-dopants, move the Fermi-level and in doing so they change the conductivity of a CBL.

Ion implanting with 43 KeV or 20 KeV creates point defects that are ineffective to make the CBL a barrier layer. This is attributed to either to n-dopants compensating the point defects and/or by the latter's association with shallow energy levels. The nature of point defects is modified, in their compensation and energy level, on ion-implanting InGaN at 53 or 63 KeV. The low leakage for the two energies, see Fig. 3.7, implies a presence of a higher blocking barrier in either case. The argument explains how blocking in CBL can be improved by changing the ion-implant energy. However, further experimental proof in support of this explanation is required. Photoluminescence measurements may need to be performed for different CBLs in a future study.

In studying apertures and CBLs with different designs and current-voltage characteristics, it is intended that on applying them in a BAVET structure one may obtain a transistor operation. The impact of different designs on the transistor operation is the focus of the section that follows.

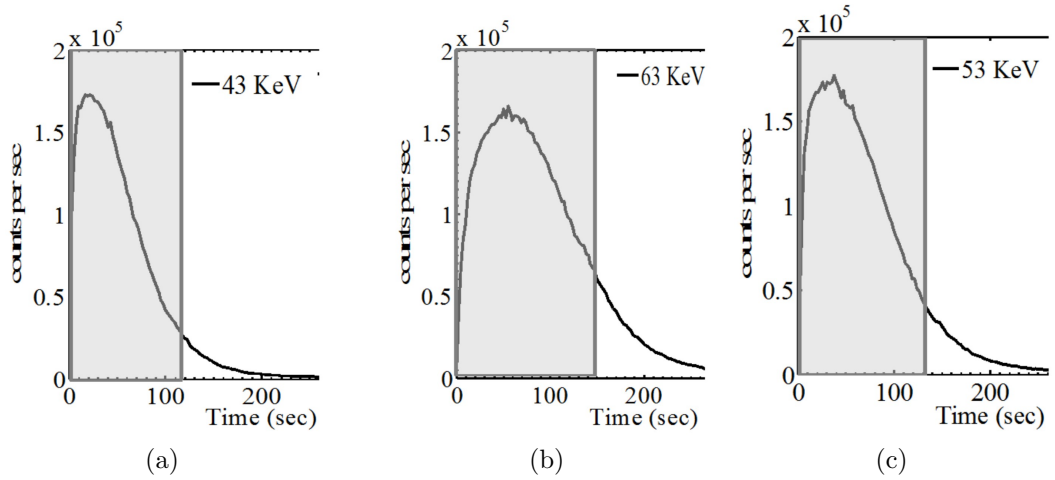


Figure 3.8: SIMS profile of Al is shown for InGaN layers that are ion-implanted at (a) 43, (b) 53 and (c) 63 KeV.

3.7 Transistor Operation in a BAVET

The reason to enhance aperture conductivity and CBL blocking is to realize transistor nature in a BAVET. We are now in a position to test a BAVET for its transistor behavior.

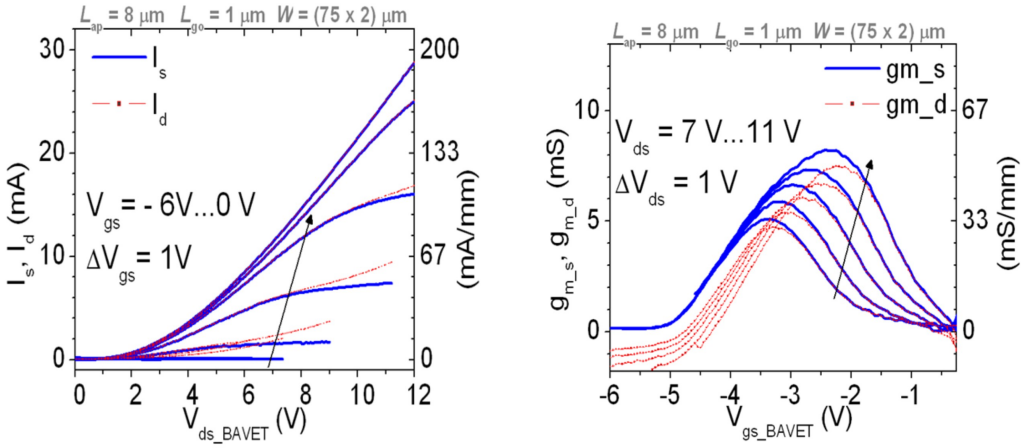
3.7.1 I_D, I_S-V_{DS}, V_{GS} Characteristics of a BAVET

BAVETs perform poorly to be treated as transistor in the cases whether the aperture is doped low and whether the CBLs are implanted at 20 KeV or 43 KeV. The poor performance is on account of low on current and high CBL leakage, respectively. Only a BAVET, which comprises an aperture that is δ-doped and a CBL that is implanted at either 53 KeV or 63 KeV, exhibits transistor functionality. This type of BAVET works as it is far from being impacted by issues of low on current and leakage. Furthermore, the similar nature of the CBLs of 53 KeV and 63 KeV translates to a similarity that their BAVETs also operate as transistors. Fig. 3.9 shows the drain (I_D) and source-current (I_S) characteristics of one such BAVET.

An on current of 200 mA.mm^{-1} is obtained (see Fig. 3.9(a)). I_S-V_{GS} measurements present a maximum g_m of 55 mS.mm^{-1} at a V_{GS} = -2.3 V. In BAVETs with 63 KeV, maximum on current and g_m, are twice as much at that of 53 KeV. Such increase in implant energy benefits g_m of the device; it is highest for 63 keV and equals 126 mS.mm^{-1}.

3.7.2 Discussion on Transistor Behavior

Reasons for g_m increasing with ion-implant energy changing from 43 KeV to 53 KeV are understood to be due to the difference in their CBL's blocking ability. But the answer to why g_m becomes twice as much for a CBL changing from 53 to 63 KeV is yet to be found. In explaining the difference in g_m for 53 KeV and 63 KeV, we suspect another phenomenon is at work. As the CBL barrier changes form 53 KeV to 63 KeV, the nature of traps at WBI and CBL region change. The change is such that it increases the channel conductivity and gate-control in L_{GO} regions and thus a higher g_m in BAVETs with 63 KeV. This phenomenon yet needs to be understood in a further investigation.



(a) (b)

Figure 3.9: (a) I_D, I_S-V_{DS}, and (b) I_D, I_S-V_{GS} characteristics measured for a BAVET with δ-doped aperture and a CBL formed by 53 KeV of ion-implantation energy. The difference in ID and IS characteristics is due to the gate leakage of device.

3.7.3 What is not achieved by design of Aperture and CBL?

Although a BAVET is shown to work as a transistor, it yet suffers in performance. Saturation ($V_{\mathrm{DS\_SAT}}$), and turn-on voltages ($V_{\mathrm{DS\_ON}}$), and output conductance (G_{OUT}) are abnormally high.

The anomalies in each parameter are discussed briefly. (a) Improved CBL design pinches off the BAVET at a threshold voltage (V_{TH}) close to -5 V. $V_{\mathrm{DS\_SAT}}$, which represents pinch-off at the drain, however, is greater than 12 V at a $V_{\mathrm{GS}} = 0$ V. $V_{\mathrm{DS\_SAT}}$ in on-state exceeds V_{TH} by more than 7 V, which is undesirable. (b) Turn-on voltage ($V_{\mathrm{DS\_ON}}$) is close to 2.5 V. It is greater than 0 V despite the elimination of InGaN-GaN barrier in δ-doped apertures. (c) Lastly, elimination of CBL leakage improves source-current saturation, and aids in mitigating G_{OUT}, but fails to make it as low as zero.

It is implied that aperture and CBL have a limited role in enhancing the performance of BAVET. It is possible that there exists a third feature that regulates $V_{\mathrm{DS\_ON}}$, $V_{\mathrm{DS\_SAT}}$ and G_{OUT}. The following section presents another experiment to eliminate anomalous nature in a BAVET, and find it's third design feature.

3.8 WBI Experiment

The experiment is referred to as WBI experiment. It is named so for reasons that will be presented shortly. The experiment comprises designing, fabricating, and characterizing BAVETs with different doping in the gate-barrier or InAlAs layer. The III-N part of the device is unchanged among the BAVETs, and each contains δ-doped aperture and 53 KeV CBL.

3.8.1 Gate-barrier doping in a Transistor

In a field-effect transistor or FET, gate-barrier has a function of bias modulating the channel. From the theory on a junction FET (JFET), doping of gate-barrier controls the gate and channel potential [5]. Any change to the doping, consequently, modifies V_{TH} and conductivity of the channel in a FET. Likewise, in a BAVET changes in certain parameters with gate-barrier doping are expected.

3.8.2 Experiment: Changing gate-barrier doping of a BAVET

The gate-barrier of InAlAs is changed in its doping from unintentional to p-type. Two of the structures are referred to as i- and p-structures (see Fig. 3.10(a) and (b)). A third structure, referred to as p-i-structure, has InAlAs doped in part as unintentional and in part as p-type. This is done such that the unintentionally doped is sandwiched between the p-doped region and the InGaAs channel (see Fig. 3.10(c)).

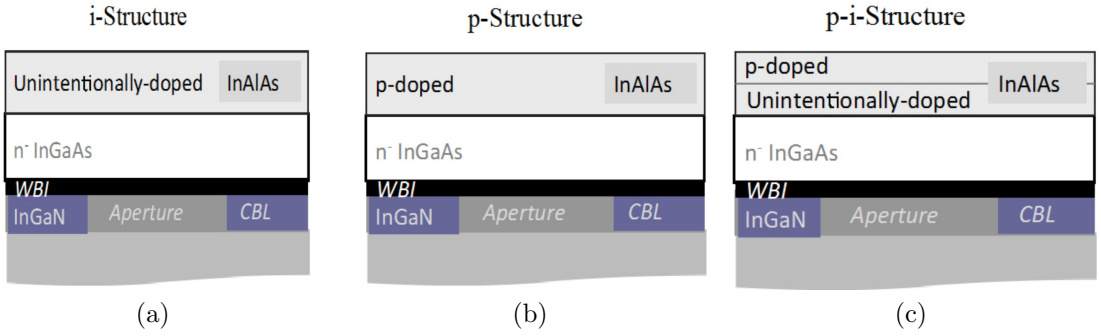


Figure 3.10: Wafer-bonded structures that differ in the doping of InAlAs are shown. (a) i-Structure comprises unintentionally doped InAlAs, (b) p-structure with p-doped InAlAs, and (c) p-i-structure containing p-doped InAlAs on top of the one that is unintentionally doped. WBI is the wafer-bonded interface in each structure.

Three III-As structures are grown, wafer-bonded to similar III-N structures, and processed to form BAVETs [10]. They are referred to as i-, p-, and p-i-BAVET.

3.9 Results and Discussion

Fig. 3.11 shows the I_{D}-V_{DS} traces of a p-i and p-BAVETs. Response of i-BAVET is that shown in Fig. 3.9(a). The three BAVETs differ in their I_{D}-V_{DS} through differences in certain parameters, namely On-resistance (R_{ON}), V_{TH}, $V_{\mathrm{DS\_ON}}$, $V_{\mathrm{DS\_SAT}}$, and G_{OUT}. What follows is an account of how these parameters (a) are derived and (b) relate to gate-barrier doping.

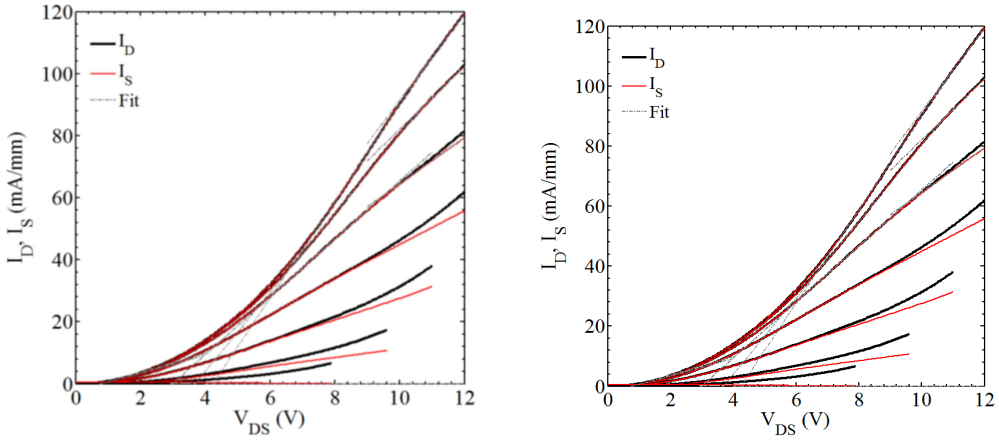


Figure 3.11: I_D, I_S-V_{DS} measurements are shown for (a) p-i, (b) p-BAVETs. V_{GS} is varied from 0 to −6 V. Linear fitting to different VGS is shown by dashed lines. Linear fitting is used to extract $V_{\mathrm{DS\_ON}}$, $V_{\mathrm{DS\_SAT}}$, R_{ON}, G_{OUT} [10].

3.9.1 Finding Medians of Device Parameters

I_{D}-V_{DS} traces are linearly fitted to extract R_{ON}, $V_{\mathrm{DS\_SAT}}$, $V_{\mathrm{DS\_ON}}$, and G_{OUT} [10]. This is identically done to I_{D}-V_{GS} traces and so is obtained V_{TH}. The median for each parameter is obtained from box-statistic on a set of devices of each type, namely i, p-i, and p-type. In the following section, the trends of median R_{ON}, V_{TH}, $V_{\mathrm{DS\_SAT}}$, $V_{\mathrm{DS\_ON}}$, and G_{OUT} vs. doping of InAlAs are presented.

3.9.2 On-resistance and Threshold voltage vs. Doping

In p-BAVETs, higher R_{ON} is observed in comparison to the other two types of BAVETs. V_{TH} experiences a change of 1 V between i- and p-BAVETs. While for i- and p-i-BAVETs, the difference in V_{TH} becomes as low as 0.2 V.

3.9.3 Turn-on, Saturation Voltages & Output Conductance vs. doping

Box $V_{\mathrm{DS\_ON}}$, $V_{\mathrm{DS\_SAT}}$, and G_{OUT} vs. InAlAs doping are shown in Fig. 3.12. $V_{\mathrm{DS\_ON}}$, $V_{\mathrm{DS\_SAT}}$ shown herein are extracted for a V_{GS} of 0 V, which is -2 V for G_{OUT}.

A characteristic is observed which is common to the three trends. Median is lowest if the BAVET comprises p-InAlAs. $V_{\mathrm{DS\_ON}}$ of 0.97 V, $V_{\mathrm{DS\_SAT}}$ of 4.48 V and G_{OUT} of 0.73 mS.mm^{-1} are the characteristics of a p-BAVET. The median $V_{\mathrm{DS\_ON}}$ and G_{OUT} peak in p-i-BAVET, whereas highest $V_{\mathrm{DS\_SAT}}$ is characteristic to i-BAVET. Similar behavior in medians vs. doping is, too, observed at other V_{GS}.

3.9.4 Discussion

The doping dependencies in R_{ON} and V_{TH} arise on account of p-doping making the channel deplete [5]. The p-doped layer is closest to the channel in p-BAVETs than in p-i-BAVETs, and so the former experiences most dramatic changes in R_{ON} and V_{TH} from that of i-BAVETs.

R_{ON} and V_{TH} behave in an expected manner with doping but that it also impacts $V_{\mathrm{DS\_ON}}$, $V_{\mathrm{DS\_SAT}}$, and G_{OUT} is an interesting event. For these are lowest in the case of p-doped InAlAs. It is confirmed that the changes in $V_{\mathrm{DS\_ON}}$, $V_{\mathrm{DS\_SAT}}$, and G_{OUT} are in response to changes in doping. How doping influences channel, on the other hand, does not explain the connection between doping and the three parameters - $V_{\mathrm{DS\_ON}}$, $V_{\mathrm{DS\_SAT}}$,

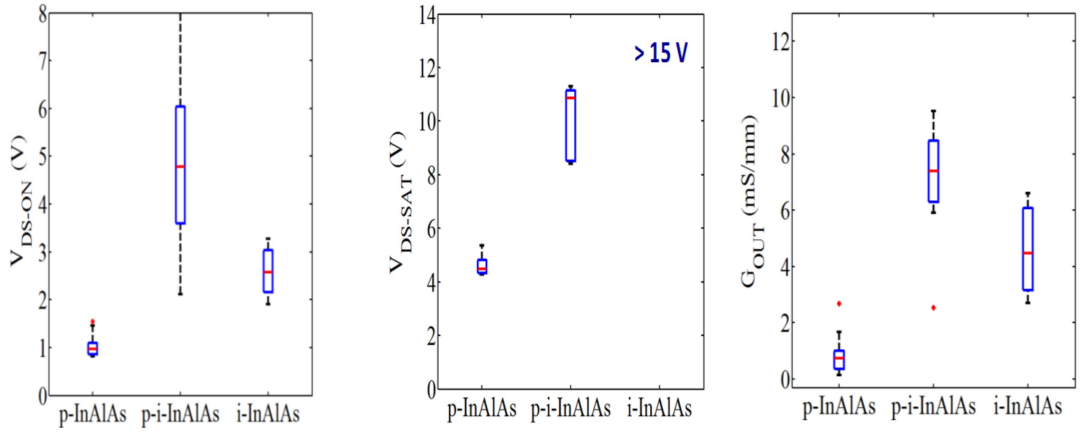


Figure 3.12: (a) $V_{\mathrm{DS\_ON}}$, (b) $V_{\mathrm{DS\_SAT}}$ and (c) G_{OUT} expressed in box-plot forms for p, p-i and i-BAVETs. Minima of $V_{\mathrm{DS\_ON}}$, $V_{\mathrm{DS\_SAT}}$ and G_{OUT} vs. InAlAs doping are obtained for a p-BAVET.

and G_{OUT}. Let us briefly explain how the change in R_{ON} or V_{TH} does not translate to similar changes in $V_{\mathrm{DS\_ON}}$, $V_{\mathrm{DS\_SAT}}$ and G_{OUT}. The differences between i-and p-BAVETs are explained.

$V_{\mathrm{DS\_ON}}$ of i- and p-BAVETs

$V_{\mathrm{DS\_ON}}$ reduces but not increases with p-doping. This implies that $V_{\mathrm{DS\_ON}}$ is not due to a barrier in the channel. It neither is from the InGaN-GaN interface, the barrier of which was eliminated by δ-doping. This leaves one region as the possible source of $V_{\mathrm{DS\_ON}}$, namely, WBI-aperture region.

$V_{\mathrm{DS\_SAT}}$ of i- and p-BAVETs

$V_{\mathrm{DS\_SAT}}$ reduces much more than the observed difference of 1 V in V_{TH} among i- and p-BAVETs. Therefore, the reduction in $V_{\mathrm{DS\_SAT}}$ is not coupled to p-doping's channel depletion. In another study, it has been found that a virtual gate at CBL-aperture edge

of WBI is what cause the difference in $V_{\mathrm{DS\_SAT}}$ and V_{TH}.

G_{OUT} of i- and p-BAVETs

Between i- and p-BAVETs, the reduction in G_{OUT} is greater than the reduction in on current or enhancement in on resistance. G_{OUT} is, therefore, suspected to reduce due to a reason different from that of channel made less conductive by p-doping. It is proposed that G_{OUT}, in fact, depends on the conductivity of the WBI-CBL interface, which is modified by gate-barrier doping. Further explanation on this subject will be part of another study.

3.9.5 How to Design WBI in a BAVET?

Detailed accounts of $V_{\mathrm{DS\_ON}}$, $V_{\mathrm{DS\_SAT}}$, and G_{OUT} vs. doping are beyond the scope of the present study. However, each parameter is shown to have a relationship to the behavior of those regions that comprise WBI.

Doping in InAlAs influences the properties of InGaAs/InGaN WBI, WBI regulates the performance of the device in more than one way, which leads us to state that WBI is another key feature of BAVETs. The feature is indirectly designed by means of doping the gate-barrier layer. The phenomenon arises in how the doping aids in passivating traps at the WBI. The details of which will be presented in another study. p-doped gate-barrier gains us a WBI that is ideal in its behavior and so obtains a near ideal BAVET.

3.10 Conclusion

Three features of a BAVET, namely, aperture, CBL and WBI were the focus of this work. Each feature was understood to regulate specific parameters of the device. The study researched different designs for each feature, and found that only certain designs

enhanced device parameters. The improvement led to the improvement in transistor characteristics of a BAVET. Explanations, on why one design worked well in comparison to others, revealed interesting phenomenon in InGaAs/InGaN BAVETs.

On current of a BAVET was determined to be based on how conductive was its aperture. n-doping the aperture with different concentrations and at different regions were experiment. High n-doping concentration, and that too if done at the InGaN-GaN interface, obtained enhanced conduction, and on current. By such δ-doping, the undesired barrier from polarization at the InGaN-GaN interface was overcome.

The design of CBL determined leakage and g_m of a BAVET. Higher energy of ion-implantation led to lower leakage and higher gm. It was proposed that the point defects from higher energy enable a higher barrier in a CBL. Ion-implantation energies of 53, and 63 KeV demonstrated the lowest leakage in comparison to 40 and 20 KeV. Additionally, the BAVET performed as a transistor for the first time and gained in g_m. It was measured to be as high as 126 mS.mm^{-1}.

The experiments on aperture and CBL led us to improved transistor behavior. $V_{\mathrm{DS\_ON}}$, $V_{\mathrm{DS\_SAT}}$, G_{OUT} were, however, further improved in the WBI experiment. The experiment of gate-barrier doping revealed its indirect impact on properties of WBI. All of the three parameters are well behaved for BAVETs with p-doped InAlAs, while unintentional doping makes the parameters behave anomalously.

Experiments on aperture doping and CBL ion-implantation energy affected the regions locally, for instance conductivity improved in aperture and blocking changed in CBL. BAVETs, however, responded to change in doping of the gate-barrier in the most unexpected manner. It impacted regions that are not only localized near the gate-barrier but also situated remotely like WBI-aperture, WBI-CBL-aperture edge and WBI-CBL.

From the knowledge on how most of the parameters, and WBI, improved with doping in gate barrier, WBI was attributed as a design feature important to the performance of

a transistor. What changes physically for the WBI is likely to be the nature of traps at WBI being modified by doping of a remote layer.

The study, thus, succeeds in (a) controlling the performance of key features of a BAVET, (b) finding the design space for aperture, CBL and WBI; (b) demonstrating InGaAs-InGaN BAVET as a transistor.

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Chapter 4

Saturation Voltage and Virtual Gate in Wafer-bonded Transistors

4.1 Introduction

Unipolar transistors, formed by wafer bonding, have required anomalously high drain voltage (V_{DS}) to obtain saturation in their drain current (I_D) characteristics [1]. The V_{DS} in consideration is referred to as the saturation voltage – V_{DS_SAT}. Switching fast and at a high voltage is one of the primary reasons to apply wafer bonding to transistor design. To this end it is necessary that a wafer-bonded transistor operate with low V_{DS_SAT}.

How V_{DS_SAT} can be controlled and what effects cause it to behave anomalously are questions, which are addressed in this manuscript. The investigation is presented over three stages. First stage describes the experiment and approach to analysis of V_{DS_SAT}. The experiment is directed to study of V_{DS_SAT} in three different device structures. An analysis approach is developed herein, which starts with identifying and experimentally deriving the fundamental constituents that formulate V_{DS_SAT}. On applying statistic to obtain a box plot of V_{DS_SAT}, its dependence on the chosen experimental devices is

revealed.

A method, which counters the anomalous phenomenon by effectively lowering $V_{\mathrm{DS\_SAT}}$ in wafer-bonded transistors, features in the second stage. The contribution of each constituent in $V_{\mathrm{DS\_SAT}}$ is brought about by the analysis and we are led to identify the key factor contributing to abnormally high $V_{\mathrm{DS\_SAT}}$ (see Fig. 4.1).

The third section performs a comparative analysis to transistors that vary in their wafer-bonded structures. The comparison is used to translate the key-contributing factor of $V_{\mathrm{DS\_SAT}}$ into a physical entity, a virtual gate. How $V_{\mathrm{DS\_SAT}}$ changes among the transistor variations, is recognized to be a response of variable behavior of virtual gate. We then arrive at an explanation of the mechanism by which the method influences $V_{\mathrm{DS\_SAT}}$.

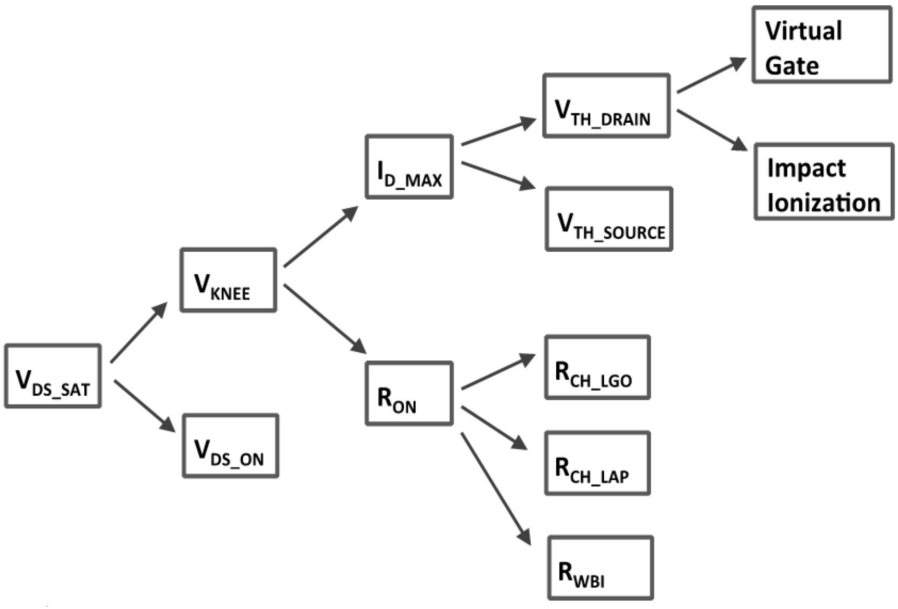

Figure 4.1: A flow chart is shown to present the approach to investigating $V_{\mathrm{DS\_SAT}}$.

Layer structure of the transistor, named as a BAVET, can be recalled from ref. [1]. A key feature of a BAVET is a wafer-bonded interface, WBI (see Fig. 4.2). For a BAVET comprising a channel in InGaAs, while the InGaN/GaN layers play the role of drift region, WBI is a transitional region between the two material systems. Both current-blocking

layer (CBL) and aperture are contained in InGaN layer (see Fig. 4.2). A barrier to enable gate-modulation is provided in the form of an InAlAs layer.

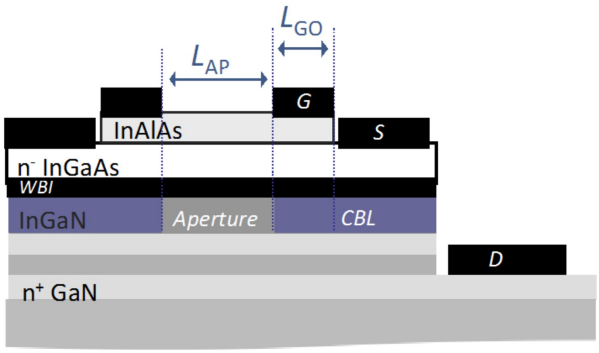

Figure 4.2: The layer structure, aperture and CBL regions are shown in a cross section schematic of a BAVET. The L_{GO} regions of InGaAs are gate-modulated while the L_{AP} region marks the aperture width, respectively. WBI denotes the wafer-bonded interface between InGaAs and InGaN. G, S, D denote the gate, source and drain electrodes of the device.

4.2 Experiment Design

An attempt is made to understand V_{DS_SAT} by means of an experiment by which the device structure is modified. A specific case of changing the doping design of InAlAs layer is investigated. The barrier layer of InAlAs in ref. [1] was designed to be a 50 nm thick and unintentionally doped InAlAs layer. Herein, the doping design of the InAlAs layer is changed in two ways: firstly, by employing p-type dopants ([Be] $= 5 \times 10^{18}$ cm^{-3}) and secondly, by variations performed to the thickness and location of the p-doped region. Total thickness of InAlAs layer is kept constant across the variations. The doping scheme is studied over three structures, one of them being similar to that in ref. [1].

Specifically, the doping scheme can be described in a statement: that the thickness of p-doped InAlAs is made to vary between 0 nm to a maximum of 50 nm in a manner such that p-doped region is brought closer to the InAlAs/InGaAs junction. In Fig. 4.3,

Table 4.1: Doping and Thicknesses Used for the Design of InAlAs in Different Structures

Structure	t_p (nm)	t_i (nm)	$t = t_p + t_i$ (nm)
p	50	0	50
$p-i$	20	30	50
i	0	50	50

the thickness of InAlAs layer is divided into two regions of thicknesses t_{p} and t_i. The thickness of p-doped region is t_{p} while t_i denotes the spacing between the p-layer and InAlAs/InGaAs junction.

Table 4.1 presents the three designs, referred to as p, p-i, and i-structures, which are distinguished by the values chosen for their t_{p} and t_i thicknesses. The dopant type is either p-type or unintentional, while the range of thickness which the p-doped region can take up ranges from 0 to 50 nm. p- and i- structures thus represent the two extremes in both the type of dopants and range of thickness. The use of a 20 nm-thick p-doped layer in the third design, named as p-i-structure, places it close to the middle in the thickness range. In addition, p-i-structure contains an unintentionally doped InAlAs as a spacer layer, which places the p-doped region 30 nm away from the InAlAs/InGaAs junction.

Fabrication processes, preceded by wafer bonding of III-Arsenide to III-Nitride (III-N), are applied in a similar fashion for each structure. BAVETs fabricated from i, p-i, and p-structures are hereinafter referred to as i, p-i and p-BAVETs.

4.3 $V_{\mathrm{DS\_SAT}}$ in BAVETs

4.3.1 $V_{\mathrm{DS\_SAT}}$ and its Constituents

An I_{D}-V_{DS} trace of a transistor can be defined to be composed of three regimes: turn-on, resistive, and saturation. Turn-on regime is defined for a V_{DS} in range of {0 V, $V_{\mathrm{DS\_ON}}$}, wherein $V_{\mathrm{DS\_ON}}$ is the minimum V_{DS} that should be applied to launch $I_{\mathrm{D}} >$

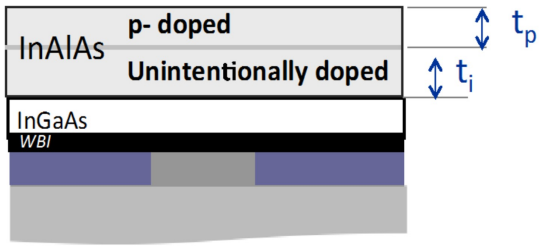

Figure 4.3: A partial cross section of a BAVET is shown to highlight the design methodology for a gate-barrier in InAlAs layer. InAlAs layer is designed to contain a p-doped region over a thickness of t_{p} and an unintentionally doped region, which acts as a spacer layer of thickness t_i. InGaAs layer is sandwiched between the InAlAs layer and WBI region.

0 mA.mm^{-1} (see Fig. 4.4). Sandwiched between the turn-on and saturation regimes is a resistive regime with lower and higher limits set at $V_{\mathrm{DS\_ON}}$ and $V_{\mathrm{DS\_SAT}}$, respectively. Saturation in I_{D} is observed for $V_{\mathrm{DS}} = V_{\mathrm{DS\_SAT}}$, a condition representative of the saturation regime. X-intercept of a line fitted to the resistive regime defines $V_{\mathrm{DS\_ON}}$. $V_{\mathrm{DS\_SAT}}$ is the X-axis component at the intersection point of two lines fitted linearly to resistive and saturation regimes. If we assume that $I_{\mathrm{D}} \approx 0$ mA.mm^{-1} for $V_{\mathrm{DS}} < V_{\mathrm{DS\_ON}}$, a relation:

$$V_{\mathrm{DS\_SAT}} = V_{\mathrm{DS\_ON}} + (I_{\mathrm{D\_MAX}} \times R_{\mathrm{ON}}) \tag{4.1}$$

can be used to represent $V_{\mathrm{DS\_SAT}}$ in terms of its constituents: $V_{\mathrm{DS\_ON}}$, R_{ON}, and $I_{\mathrm{D\_MAX}}$. One could determine on resistance, R_{ON}, and maximum current, $I_{\mathrm{D\_MAX}}$, from the resistive and saturation regimes, respectively in the manner shown in Fig. 4.4.

Values for $V_{\mathrm{DS\_SAT}}$, $V_{\mathrm{DS\_ON}}$, V_{SAT} are medians derived from respective box plots. Box statistics is performed on I_{D}-V_{DS} traces measured at $V_{\mathrm{GS}} = 0$ V.

4.3.2 Necessity of using Statistics

When measuring devices across a die or a wafer, a spread in their response can exist. It can arise from non-uniformities pertaining to their growth or fabrication processes.

Such a spread in response can be made worse in wafer-bonded devices, which owe their operation to electrical conduction through WBI. Applying statistics to a data set is therefore deemed necessary to separate unreal trends from authentic phenomena and accurately examine the behavior of such wafer-bonded devices. Thus, in this work, experimental data is first processed using box-plot statistic, analyzed and understood by the use of medians.

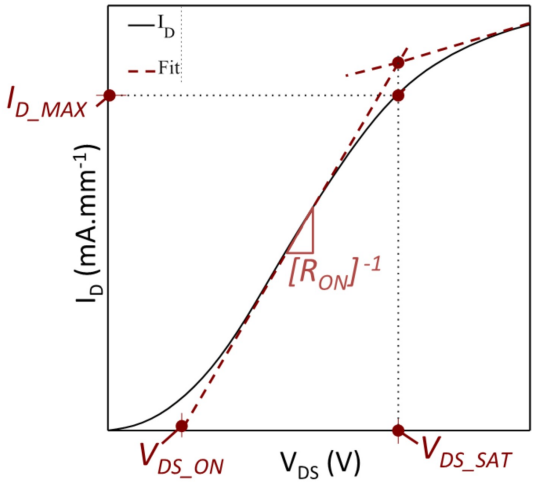

Figure 4.4: I_{D}-V_{DS} characteristics of a BAVET measured for a V_{GS}. The experimentally measured trace is shown by a solid line, which is linearly fitted. The fitted traces are plotted in dashed-line form. $V_{\mathrm{DS\_ON}}$ is the x-intercept of the intersection point of V_{DS} axis and the line fitted in linear regime. The intersection point of lines, fitted to linear and saturation regimes, denotes $V_{\mathrm{DS\_SAT}}$ in the x-intercept while the y-intercept represents $I_{\mathrm{D\_MAX}}$. R_{ON} is expressed by inverse of the slope in linear regime.

4.4 Approach to Analysis

The analysis procedure is described in the following steps.

(i) BAVETs are operated under DC bias and room temperature conditions. Fig. 4.5 presents the measured I_{D}-V_{DS} responses of i, p-i, and p-BAVETs.

(ii) $V_{\mathrm{DS\_SAT}}$ can then be derived, from the I_{D}-V_{DS} trace, at any applied V_{GS} in the

manner shown in Fig. 4.4. For an example case shown herein, a V_{GS} of 0 V is chosen.

(iii) Additional BAVETs, belonging to each structure, are characterized for their V_{DS_SAT} in above mentioned conditions. Specifically, 13 devices in each structure are examined for their I_D-V_{DS} response.

(iv) The analysis is taken further by representing the extracted values of V_{DS_SAT} in form of a box plot (see Fig. 4.6). V_{DS_SAT} can then be expressed by the median of the box as long as the standard deviations remain much less than the median. Standard deviation is the extent by which the upper or lower limit of the box is separated from the median line (see Fig. 4.6).

(v) Box plots of V_{DS_SAT}, when derived for different device designs, can be compared for underlying trends (see Fig. 4.6).

The scope of this manuscript analyzes box V_{DS_SAT} for three structures differing in their doping of InAlAs. Extraction of median V_{DS_SAT} in i-BAVETs is made difficult, as only a hint of saturation behavior is evident in their I_D-V_{DS} characteristics at $V_{GS} = 0$ V (see Fig. 4.5(a)). Applying V_{DS} greater than 20 V is required for an accurate extraction of V_{DS_SAT}. The parameter analyzer limits operating at such high voltages, leading to a scarcity of data for i-BAVETs. As a result box plot V_{DS_SAT} for i-BAVETs is absent from Fig. 4.6 and we are led to assume the median to be greater than 15 V.

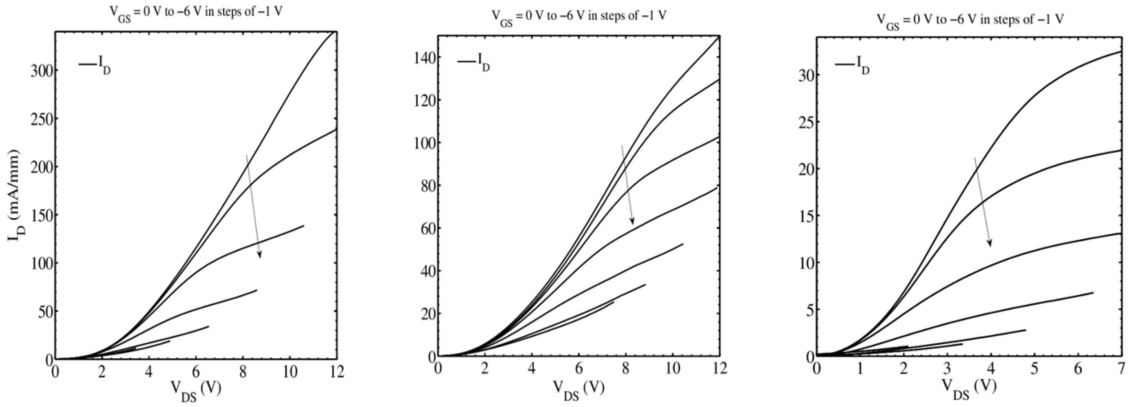

Figure 4.5: I_{D}-V_{DS} characteristics measured for (a) i, (b) p-i- and (c) p-BAVETs.

4.5 $V_{\mathrm{DS\_SAT}}$ in Bavets and Doping in InAlAs

4.5.1 Is $V_{\mathrm{DS\_SAT}}$ affected by a variation performed to device structure, especially doping in InAlAs?

On arranging box plots of $V_{\mathrm{DS\_SAT}}$ against the doping in InAlAs, a strong dependence of $V_{\mathrm{DS\_SAT}}$ on the latter is implied (see Fig. 4.5). The median of $V_{\mathrm{DS\_SAT}}$ follows a trend by which it increases in the order of p-, p-i, i-structure. It can conversely be stated: $V_{\mathrm{DS\_SAT}}$ reduces when traced in the reverse order. A methodology is thus revealed by which $V_{\mathrm{DS\_SAT}}$ can be controlled in BAVETs. The basis of this methodology lies in the design of the layer structure. Understanding the mechanism by which the method works is thus worth investigating.

4.5.2 $V_{\mathrm{DS\_ON}}$ vs. Doping in InAlAs

An earlier section described two factors: $V_{\mathrm{DS\_ON}}$, and R_{ON} times $I_{\mathrm{D\_MAX}}$ that add up to determine $V_{\mathrm{DS\_SAT}}$. Investigating the influence of doping on $V_{\mathrm{DS\_ON}}$ becomes the starting point in seeking the mechanism behind the relationship of doping and $V_{\mathrm{DS\_SAT}}$.

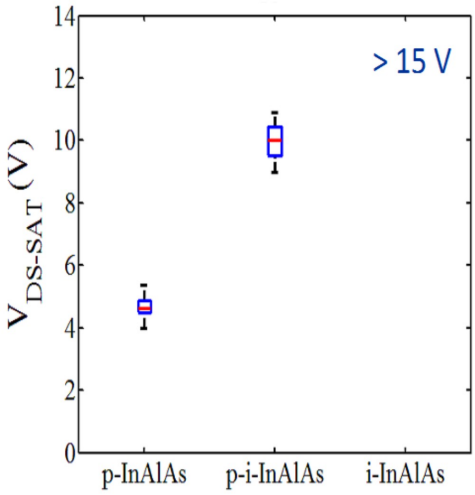

Figure 4.6: Box $V_{\text{DS\_SAT}}$ is shown as a function of doping in InAlAs. For each box, the red line denotes the median while the upper and lower limits of standard deviation are denoted by the top and bottom edges of the box. Box data for i-BAVETs is unavailable but approximately estimated to be greater than 15 V. Median increases monotonically in the order of p-, p-i-, and i-BAVETs.

Table 4.2: $V_{\text{DS\_SAT}}$, $V_{\text{DS\_ON}}$ and V_{SAT} for Different Bavet Structures

BAVET Structure	$V_{\text{DS\_SAT}}$ (V)	$V_{\text{DS\_ON}}$ (V)	V_{KNEE} (V)
p	4.6	1.08	3.608
$p-i$	10	4	6.51
i	> 15	2.8	> 12 V

When the analysis approach, described in Section 4.4, is applied to derive box plot $V_{\text{DS\_ON}}$ vs. doping in InAlAs, a bell shaped trend is witnessed, the maxima of which occurs for p-i-BAVET (see Fig. 4.7).

4.5.3 Contributions of $V_{\text{DS\_ON}}$ to $V_{\text{DS\_SAT}}$

Table 4.2 lists $V_{\text{DS\_SAT}}$ and $V_{\text{DS\_ON}}$ for each type of BAVET. It is observed that for each BAVET $V_{\text{DS\_ON}}$ has a minor contribution to $V_{\text{DS\_SAT}}$. In performing subtraction of $V_{\text{DS\_SAT}}$ and $V_{\text{DS\_ON}}$, the primary contributor, referred to as V_{KNEE}, is obtained (see Table 4.2). From the fact that V_{KNEE} is equivalent to the product term in (4.1), it can

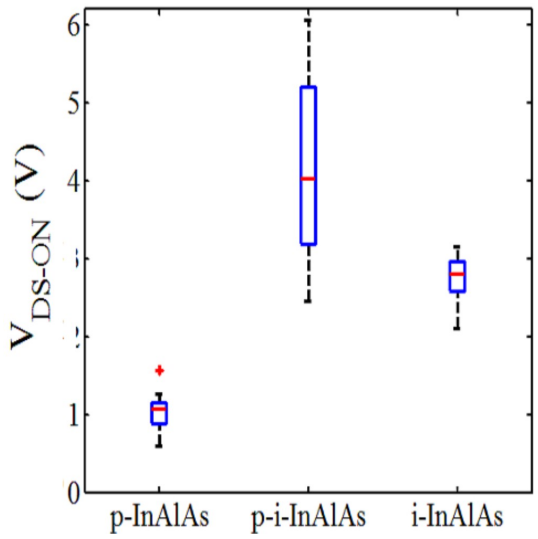

Figure 4.7: $V_{\mathrm{DS\_ON}}$ expressed in its box-plot form for p, p-i and i-BAVETs. A bell shaped trend is depicted in $V_{\mathrm{DS\_ON}}$ vs. InAlAs doping.

then be suggested that $V_{\mathrm{DS\_SAT}}$ is majorly on account of V_{KNEE} and its constituents: $I_{\mathrm{D\_MAX}}$ and R_{ON}.

The dependence of $V_{\mathrm{DS\_ON}}$ on doping in InAlAs implies another important aspect about $V_{\mathrm{DS\_SAT}}$. The bell shaped dependence between $V_{\mathrm{DS\_ON}}$ and doping is relatively weaker than the latter's incremental effect on $V_{\mathrm{DS\_SAT}}$ (see Fig 4.7). Therefore, $V_{\mathrm{DS\_ON}}$, with its dependence on doping, does not solely furnish the changes brought in $V_{\mathrm{DS\_SAT}}$. For the change must then be primarily absorbed through variations caused in V_{KNEE}. The trend in V_{KNEE} is evident from its box vs. doping plot shown in Fig. 4.8. We proceed, in this study of the origin of anomalous $V_{\mathrm{DS\_SAT}}$, by investigating on why V_{KNEE} monotonously increases in the order of p, p-i, i-BAVETs (see Fig. 4.8).

Values for V_{KNEE}, R_{ON} and $I_{\mathrm{D\_MAX}}$ are medians derived from respective box plots. Box statistics is performed on I_{D}-V_{DS} traces measured at $V_{\mathrm{GS}} = 0$ V.

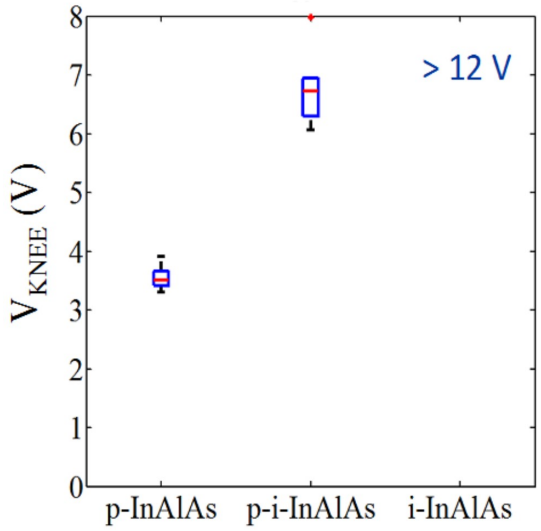

Figure 4.8: Box V_{KNEE} vs. doping in InAlAs, wherein the difference of $V_{\mathrm{DS\_SAT}}$ and $V_{\mathrm{DS\_ON}}$ is assigned to V_{KNEE}. Varying p- to i-doping, through p-i-doping, in BAVETs enhances V_{KNEE}.

4.6 Re-Evaluating I_{D}-V_{DS}

4.6.1 Method to Remove Turn-On Characteristic from I_{D}-V_{DS}

Now that $V_{\mathrm{DS\_ON}}$ has been shown to be inconsequential to high $V_{\mathrm{DS\_SAT}}$, V_{KNEE} becomes the primary means to analyze $V_{\mathrm{DS\_SAT}}$. Exclusion of turn-on regime from I_{D}-V_{DS} is then the next logical step.

I_{D}-V_{DS} needs to be re-evaluated such that it is devoid of the turn-on regime but comprises both linear and saturation regimes. The linear regime traces I_{D} as a function of V_{DS} from $V_{\mathrm{DS}} = 0$ V to V_{KNEE} V. It is evaluated as:

$$I_D = V_{\mathrm{DS}}/R_{\mathrm{ON}} \tag{4.2}$$

The saturation regime, spanning for $V_{\mathrm{DS}} > V_{\mathrm{KNEE}}$, is obtained for an ideal case of infinite output resistance (R_{OUT}) or constant I_{D} – $I_{\mathrm{D\_MAX}}$. $I_{\mathrm{D\_MAX}}$ can be obtained in either the

Table 4.3: V_{KNEE}, R_{ON} and $I_{\mathrm{D\_MAX}}$ for Different Bavet Structures

BAVET Structure	V_{KNEE} (V)	R_{ON} (Ω.mm)	$I_{\mathrm{D\_MAX}}$ (mA.mm)
p	3.608	138	25.4
p-i	6.51	59	106
i	>12	58	-

manner depicted in Fig. 4.4 or by means of the following relation:

$$I_{\mathrm{D\_MAX}} = V_{\mathrm{VNEE}}/R_{\mathrm{ON}} \tag{4.3}$$

Medians derived from box of both R_{ON} and V_{KNEE} are employed in (4.2) and (4.3).

4.6.2 Output Resistance in the Analysis of V_{KNEE}

The condition that R_{OUT} is infinite is obviously not the case observed in any of the BAVETs shown in Fig. 4.4. A possibility then arises by which V_{KNEE} is modifiable on account of InAlAs doping influencing R_{OUT}. Let us first identify how R_{OUT} changes with doping and whether it influences V_{KNEE}. The answer to these questions may indicate on the correctness of treating R_{OUT} as infinite in (4.3).

From another ongoing study, R_{OUT} is observed to remain unchanged in p-i and i-BAVETs, despite the large variation in their V_{KNEE}. It is thus argued that two unrelated phenomena cause such contrasting behavior in V_{KNEE} and R_{OUT}. This is regarded as a preliminary sign of V_{KNEE} being weakly coupled to R_{OUT}. If we consider the simplest case of R_{OUT} being infinite, the consistency of the analysis is unharmed, thus validating the assumption. Likewise, it can be stated that V_{KNEE} is unaffected from the non-idealities of saturation regime. The argument works in support of replacing the experimentally measured saturation regime with one derived by (4.3).

4.6.3 I_D-V_{DS} for i, p-i, p-BAVETs

The above mentioned method that generates I_D-V_{DS}, minus turn-on characteristics, is applied to each BAVET type. R_{ON} and V_{KNEE} values for p, p-i, i-BAVETs are listed in Table 4.3. These values pertaining to $V_{GS} = 0$ V when used in Table 4.2 and Table 4.3 result in an I_D-V_{DS} representation of a BAVET. Such I_D-V_{DS} traces are derived for each type of BAVET and shown in Fig. 4.8.

Since the saturation regime, like turn-on regime, has little significance to the study of V_{DS_SAT}, we can scarcely avoid the inference that the factor leading to anomalous V_{DS_SAT} must have its origin in the linear regime. In particular, we may next examine R_{ON} and I_{D_MAX}.

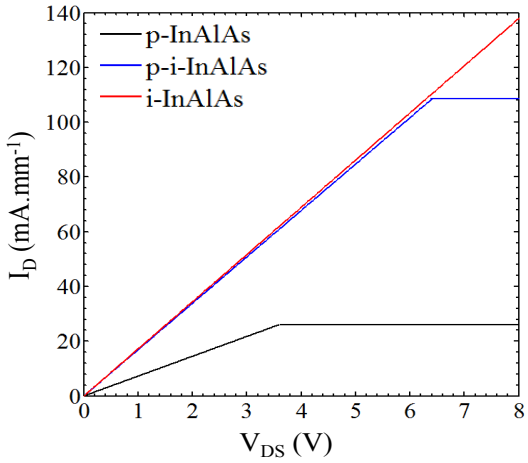

Figure 4.9: I_D-V_{DS} traces when re-evaluated with the turn-on regime absent and saturated regime shown as an ideal case of constant current. I_D-V_{DS} traces are shown for BAVETs with different doping in InAlAs. Linear regimes of p- and p-i-BAVETs follow each other on account of similar R_{ON}.

4.7 Role of R_{ON} and I_{D_MAX} in V_{KNEE}

The exact manner of how the change in V_{KNEE} takes place is investigated by the aid of studying R_{ON} and I_{D_MAX}. We begin with the case of doping type changing from

unintentional (referred to as i-doping) to p-i-doping.

4.7.1 Change doping in InAlAs from i- to p-i-type

Let us compare the I_{D}-V_{DS} traces of i- and p-i-BAVETs (see Fig. 4.9). The impact of applied doping change on V_{KNEE}, R_{ON}, $I_{\mathrm{D\_MAX}}$ can be represented by the relations:

$$(V_{\mathrm{KNEE}})_i > (V_{\mathrm{KNEE}})_{p-i} \tag{4.4}$$

$$(R_{\mathrm{ON}})_i > (R_{\mathrm{ON}})_{p-i} \tag{4.5}$$

$$(I_{\mathrm{D\_MAX}})_i > (I_{\mathrm{D\_MAX}})_{p-i} \tag{4.6}$$

The fact that R_{ON} remains unchanged, with respect to the change of i- to p-i-doping, reveals interesting information that the reduction in V_{KNEE} is brought on by $I_{\mathrm{D\_MAX}}$. On the other hand, influence of doping on $I_{\mathrm{D\_MAX}}$ does not conform to that on R_{ON}.

To understand on how this phenomenon, which makes R_{ON} unrelated to $I_{\mathrm{D\_MAX}}$, comes about, it is necessary to take the recourse of threshold voltage (V_{TH}) of the transistor. A brief background on the relationship of R_{ON} and $I_{\mathrm{D\_MAX}}$ to V_{TH} follows.

$V_{\mathrm{TH,SOURCE}}$ in a BAVET

V_{TH}, from the theory of field-effect transistors (FET) is the voltage needed to pinch off the channel at the source electrode. Hereinafter, it is referred to as $V_{\mathrm{TH,SOURCE}}$in BAVETs, for which the pinch off occurs at the source and in L_{GO} region when $V_{\mathrm{GS}} = V_{\mathrm{TH,SOURCE}}$. Just as the electrostatics, that arises from the doping of gate-barrier and channel layers, determines V_{TH} of a junction FET, likewise $V_{\mathrm{TH,SOURCE}}$ depends on doping of InGaAs and InAlAs layers in BAVETs.

R_{ON} in a BAVET

Let us first briefly discuss R_{ON} in a FET. It is defined by the inverse of channel conductivity, wherein channel conductivity is a function of (V_{GS}-V_{TH}). If we fix V_{GS} such that FET is in its on state, then R_{ON} can be made high or low by shifting V_{TH} negative or positive, respectively. The analogous connection between a FET and a BAVET exists in the concept of R_{ON} and $R_{CH,LGO}$. There are additional components to R_{ON} of a BAVET, which arise in the aperture – $R_{CH,LAP}$, WBI – R_{WBI} and drift regions (see Fig. 4.10). R_{ON} may be studied in parts through the expected behavior of its components.

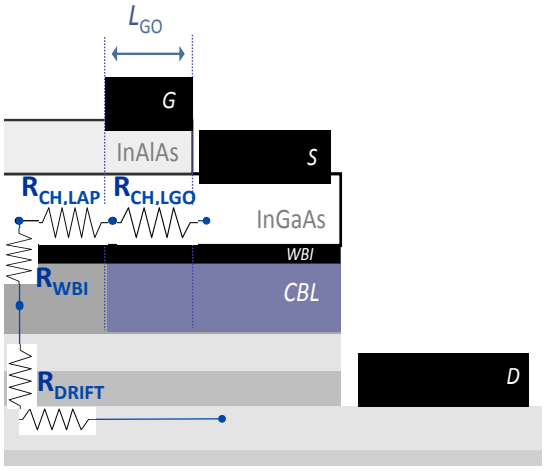

Figure 4.10: The components of R_{ON} are superimposed on a cross-section schematic of a BAVET. $R_{CH,LGO}$ and $R_{CH,LAP}$ denote the resistance offered in the L_{GO} and aperture regions of the channel. WBI is associated with a resistance - R_{WBI}, while the resistance of the region located between WBI and drain electrode is denoted by R_{DRIFT}.

Methods to Estimate Different Components of R_{ON}

$R_{CH,LAP}$ and R_{WBI} are directly related to the charge profile in L_{AP} regions of channel and WBI regions, respectively. Information on charge distribution is deducible from capacitance-voltage measurements (C-V). Along with C-V, measurement results of transmission line method (TLM) are used in estimating channel conductivity in the L_{GO}

regions, inverse of which is referred by $R_{\mathrm{CH,LGO}}$ (see Fig. 4.10).

Components of R_{ON} vs. doping in InAlAs

Two components of R_{ON} that directly depend on the electrostatics induced by the doping in InAlAs are: $R_{\mathrm{CH,LGO}}$, $R_{\mathrm{CH,LAP}}$. These resistive components are classified in the parts of channel overlaying aperture and CBL regions, respectively (see Fig. 4.10). BAVETs that comprise same doping in their channels but vary in their doping for InAlAs consequently differ in $V_{\mathrm{TH,SOURCE}}$, $R_{\mathrm{CH,LGO}}$ and $R_{\mathrm{CH,LAP}}$.

R_{WBI} bears an indirect dependence in a case when doping in InAlAs impacts the trap response at WBI, the discussion of which will be subject of another study on field-plate. R_{DRIFT} can also influence R_{ON}. The drift region, because it extends from extends from WBI to drain-electrode and comprises of III-N layers, it remains unaffected by what doping is applied to InAlAs (see Fig. 4.10). It is then correct to assume that the resistivity of the drift does not contribute in changing R_{ON} when varying doping of InAlAs.

How R_{ON} is unchanged despite the doping change of i- to p-i?

Let us first find the nature of R_{ON}, which renders it independent of the doping change. Sheet resistance of channel in L_{GO} regions is measured to be 416 and 466 Ohms/sq^{-1} for i- and p-i-structures, respectively. There are two things to notice in the C-V data shown in Fig. 4.11. Firstly, it confirms that the channel in i-structure is doped to 4×10^{17} cm^{-3}, which is 1.3 times as much as that of p-i-structure. The second observation relates to the depletion region profiles in each of the structure. In each of the two, channel is undepleted near the InAlAs/InGaAs junction while it is similarly depleted in regions near the InGaAs/CBL junction. It is inferred that the thickness of undepleted channel is same in both i and p-i structures.

There are two possible factors rendering the ineffectiveness of p-doped layer in deplet-

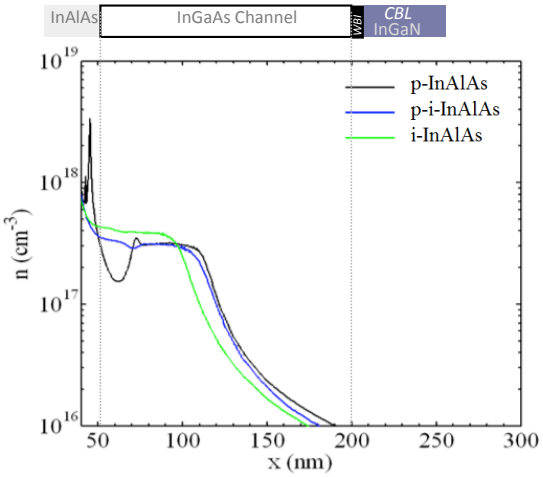

Figure 4.11: Apparent charge profile n(x) vs. depth shown for each of three structures. The extraction of n(x) utilizes a C-V trace measured at an oscillation frequency of 1 MHz. The locations of InAlAs/InGaAs and InGaAs/WBI interfaces are marked based on the expected thicknesses of InAlAs and InGaAs layers.

ing the channel at InAlAs/InGaAs junction of p-i-BAVET. One factor is that p-layer is partly depleted by surface charges. Other reason is the spacer layer of i-InAlAs absorbs the electrostatics arising from ionized p and n dopants in InAlAs and InGaAs layers, respectively, which causes negligible depletion width in InGaAs channel.

The reasons behind the depletion at InGaAs/CBL are currently under investigation. The above mentioned observations illustrate that L_{GO} region of channels in both the structures follow each other closely. When following on an assumption that the mobility and thickness of the channel are unchanged in the two structures, then the ratio of doping concentration closely matches the inverse of the ratio of their sheet resistances. This secures an explanation on why both the structures show a minor difference in their sheet resistances. The experimental data further implies a weak dependence of $R_{\mathrm{CH,LGO}}$ on the two doping types. $R_{\mathrm{CH,LAP}}$ can not be accurately extracted from TLM, yet in depicting similar charge profiles by C-V, $R_{\mathrm{CH,LAP}}$ and InAlAs are made independent of each other as well.

$V_{\mathrm{TH,SOURCE}}$ extracted from I_{D}-V_{GS} traces are observed to differ between 0.2 to 0.4 V in

the two cases. This small change in $V_{\mathrm{TH,SOURCE}}$ is expected from the constancy observed in $R_{\mathrm{CH,LGO}}$. The reason for R_{ON} being independent of the doping in Fig. 4.9 is proven to be due to $R_{\mathrm{CH,LGO}}$ staying constant in either case. This simplifies the treatment of R_{ON} in assuming that it comprises mainly of $R_{\mathrm{CH,LGO}}$, with no or little contribution from $R_{\mathrm{CH,LAP}}$, R_{WBI}, R_{DRIFT}. This treatment will find more support in the study of $V_{\mathrm{DS\_SAT}}$ vs. field plate.

An earlier statement inferred that $I_{\mathrm{D\_MAX}}$, and not R_{ON}, led to anomalously high V_{KNEE}. The above mentioned discussion provides an additional knowledge that $V_{\mathrm{TH,SOURCE}}$ is scarcely changing with doping variation of i to p-i-type. The change in V_{KNEE}, on account of the doping change of i to p-i-type, is understood to be not caused through $V_{\mathrm{TH,SOURCE}}$.

$I_{\mathrm{D\_MAX}}$ and its relationship with $V_{\mathrm{TH,DRAIN}}$

$I_{\mathrm{D\_MAX}}$ is the maximum drain-current when the channel has pinched-off at the drain-edge of the channel. Conventional transistors, whether designed to follow gradual channel approximation or velocity saturation, exhibit V_{KNEE} by the relation:

$$V_{\mathrm{KNEE}} \leq V_{\mathrm{GS}} - V_{\mathrm{TH,DRAIN}} \tag{4.7}$$

wherein, $V_{\mathrm{TH,DRAIN}}$ is the threshold voltage of the channel at the drain-end of the channel, and is equivalent to threshold voltage of the transistor measured at the source. So, in the case when:

$$V_{\mathrm{TH}} = V_{\mathrm{TH\_DRAIN}} - V_{\mathrm{TH,SOURCE}} \tag{4.8}$$

V_{KNEE} may only change by means of (4.7) through V_{GS} and $V_{\mathrm{TH,DRAIN}}$.

What mechanism varies $I_{\mathrm{D\_MAX}}$ and corresponding V_{KNEE} for the doping change?

In BAVETs, drain-edge is defined in the region comprising CBL/Aperture edge of the channel. For i- and p-i-BAVETs shown in Fig. 4.9, V_{GS} is set at 0 V, and it is known that $V_{\mathrm{TH,SOURCE}}$ is constant for i- and p-i-doping types. Two theories about $V_{\mathrm{TH,DRAIN}}$ and V_{KNEE} are then proposed: (a) V_{KNEE} must change by means of variation in $V_{\mathrm{TH,DRAIN}}$ and (b) $V_{\mathrm{TH,DRAIN}}$ and $V_{\mathrm{TH,SOURCE}}$ are not equivalent. Eqn. (4.8) is not applicable in BAVETs. It can further be stated that R_{ON} and $I_{\mathrm{D\_MAX}}$ are weakly coupled, because their respective control knobs: $V_{\mathrm{TH,SOURCE}}$ and $V_{\mathrm{TH,DRAIN}}$, are independent of each other. By the proposed two theories, a deduction is made that $V_{\mathrm{TH,DRAIN}}$changes by a larger magnitude than $V_{\mathrm{TH,SOURCE}}$as the doping changes from i- to p-i-type and results in both the observed doping-related trend and anomalous nature of V_{KNEE}.

4.8 Physical Origin of Anomalous $V_{\mathrm{TH,DRAIN}}$

We are in a position to interpret the physical process behind the phenomenon of decoupled $I_{\mathrm{D\_MAX}}$ and R_{ON} or $V_{\mathrm{TH,DRAIN}}$ and $V_{\mathrm{TH,SOURCE}}$. There are two possibilities in determining the physical origin leading to high $V_{\mathrm{TH,DRAIN}}$. The following sections first propose two physical mechanisms and then reasons to bring out the primary physical process leading to anomalous nature of all three: $V_{\mathrm{TH,DRAIN}}$, V_{KNEE}, $V_{\mathrm{DS\_SAT}}$.

4.8.1 How can the dependence be modeled physically?

Impact ionization and the presence of a virtual gate are possible suspects which can change the electrostatic potential near the drain-edge of the channel and cause variations to $V_{\mathrm{TH,DRAIN}}$.

Impact ionization

In ref. [1], BAVETs with i-InAlAs suffered from impact ionization related weak pinch-off in the I_D-V_{DS} response. The pinch off was especially worse near the off state. Off state refers to those I_D-V_{DS} traces, which are measured for a V_{GS} in the range of -4 V to -6 V. In this study of V_{DS_SAT}, the analysis is restricted to the on-state regime of V_{GS}, wherein it varies from 0 V to -3 V. So it is necessary to find the factors impacting on state performance. Ref. [1] does not settle the question of whether impact-ionization also weakens the pinch-off in on state. Let us briefly illustrate herein on this question, because if the answer hints to the absence of impact ionization then the latter can be eliminated as the physical reason of high $V_{TH,DRAIN}$.

A common way to detect impact-ionization is if the I_D-V_{DS}, V_{GS} or Drain-current injection measurements show positive-temperature coefficient [2], [3]. Temperature coefficient is positive when breakdown voltage increases as temperature increases. Positive temperature coefficient can also be expressed in I_D increasing with temperature, for a given V_{DS} or V_{GS} in I_D-V_{DS} or V_{GS} responses, respectively. For the present investigation temperature dependent I_D-V_{DS}, V_{GS} measurements in i-BAVET have shown that while I_D shows a positive temperature coefficient in the off-state regime, on-state characteristics present a negative coefficient. This property in on state eliminates the possibility of impact-ionization. Utilizing this property, we propose that impact-ionization is not the physical factor by which $V_{TH,DRAIN}$ or V_{KNEE} are made high in i-BAVETs in comparison to p-i-BAVETs.

Buried Virtual Gate in BAVETs

The experimental trends depicted in eqn. (4.4)-(4.6) represent another significant fact. Let us imagine a transistor with a back-gate. In Fig. 4.9, the I_D-V_{DS} traces pertaining

to i and p-i-BAVETs have parallelism offered in the situation wherein a transistor is measured first in the presence and then in the absence of a back-gate. A specific case of a back-gated transistor is when back-gating the transistor imposes a shift in $V_{\mathrm{TH,DRAIN}}$ without altering R_{ON}.

We are now in a position to interpret (4.4)-(4.6) and the corresponding I_{D}-V_{DS} traces in Fig. 4.9. They are caused by a back-gate residing at the CBL/Aperture edge of the channel, which also happens to be located in the proximity of WBI. This is a localized buried back-gate in a BAVET, and hereinafter, is referred to as virtual gate. Virtual gate is especially dominant in i-BAVETs and it is that which causes their $V_{\mathrm{DS\_SAT}}$ to be high in comparison to p-i-BAVETs. Physically modeling the virtual gate and precisely identifying its location in BAVET need to be addressed. These aspects will be dealt with as part of ongoing studies on the influence of applied bias, field-plating and aperture width on virtual gate.

4.9 V_{KNEE} and Virtual Gate vs. Doping

Having identified virtual gate to be the physical origin of abnormal V_{KNEE} in i-BAVETs and that it becomes less effective on changing the doping to p-i-type, let us check if similar reasoning suffices to explain the behavior of p-i- and p-BAVETs.

4.9.1 Change doping in InAlAs from p-i- to p

From Table 4.2 it is known that lowest V_{KNEE} is obtained in p-BAVETs. Comparison of p-i and p-BAVETs (see Fig. 4.9) gives way to relations:

$$(V_{\mathrm{KNEE}})_{p-i} > (V_{\mathrm{KNEE}})_{\mathrm{p}} \tag{4.9}$$

$$(R_{\mathrm{ON}})_{p-i} < (R_{\mathrm{ON}})_{\mathrm{p}} \tag{4.10}$$

$$(I_{\mathrm{D\_MAX}})_{p-i} > (I_{\mathrm{D\_MAX}})_{\mathrm{p}} \tag{4.11}$$

Reduction of V_{KNEE}, in the order of p-i and p, is accompanied by a similar trend in $I_{\mathrm{D\_MAX}}$. However, (4.10), which behaves in contrast to that in (4.5), suggests R_{ON} additionally impacts the change in V_{KNEE}.

How R_{ON} changes with the doping change of i- to p-i?

In the discussion on p-i-BAVETs in Section 4.7, C-V measurements implied that the p-doped layer separated by a i-doped region has little consequence in depleting n-doped InGaAs channel. The depletion width in the channel, however, increases if the thickness of p-doped layer is increased such that p-doped layer is brought closer to the InAlAs/InGaAs junction by replacing the i-doped region of InAlAs with p-doped. InAlAs designed using the above mentioned principle brings us to the p-BAVET described in Table 4.1, which is expected to have a larger depletion width in the channel than that in p-i-BAVETs.

C-V shows a channel with less available charge in p-BAVETs relative to that of p-i-BAVET (see Fig. 4.11). An additional drop in mobility further enhances sheet resistance in p-BAVET. Higher depletion region in p-BAVETs, which is in contrast to p-i-BAVETs, is the principal cause of the trend shown by R_{ON} in (4.10). Difference in the depletion electrostatics of the two types of BAVETs is expressed in their $V_{\mathrm{TH,SOURCE}}$ measurements.

$V_{\mathrm{TH,SOURCE}}$ differs by -1 V between p- to p-i-BAVETs.

What Mechanism Varies $I_{\mathrm{D\_MAX}}$ and V_{KNEE} for the Doping Change?

In understanding V_{KNEE} by comparison of p-i and p-BAVETs, we must consider whether the behavior described by (4.9) is purely a resultant of the difference in $V_{\mathrm{TH,SOURCE}}$.

From Table 4.3 one can estimate that V_{KNEE} increases by 2.9 V when doping changes from p-i to p-type. The respective values for $V_{\mathrm{TH,DRAIN}}$ are obtained by imposing equality condition in (4.7). Under the condition of $V_{\mathrm{GS}} = 0$ V, it is ascertained that $V_{\mathrm{TH,DRAIN}}$ varies, as a function of doping, by the same magnitude as the change in V_{KNEE}.

The discrepancy of $V_{\mathrm{TH,DRAIN}}$ and $V_{\mathrm{TH,SOURCE}}$ undergoing a change by different magnitudes for the given change in doping, suggests V_{KNEE} changes through both $V_{\mathrm{TH,DRAIN}}$ and $V_{\mathrm{TH,SOURCE}}$. And the fact that doping modifies $V_{\mathrm{TH,DRAIN}}$ by an additional 1.9 V than it does $V_{\mathrm{TH,SOURCE}}$ highlights that the contribution of $V_{\mathrm{TH,DRAIN}}$ dominates V_{KNEE}.

Does Virtual Gate Theory Suffice to Explain change in $V_{\mathrm{DS\_SAT}}$ from p-i- to p-type?

The case of $V_{\mathrm{TH,DRAIN}}$ and $V_{\mathrm{TH,SOURCE}}$ being unequal is recurrent and similar to the discussion of Section 4.7, wherein the doping was changed from i- to p-i. We reapply the thought process developed for the doping change of i- to p-i-type to further state that R_{ON} and $I_{\mathrm{D\_MAX}}$ are dominantly decoupled by the presence of a virtual gate when doping changes from p-i- to p-type. Virtual gate resides in p-i-BAVETs but its impact on V_{KNEE} is weakest for p-BAVETs. The theory of virtual gate suffices to explain what causes V_{KNEE} to reduce from p-i- to p-BAVETs.

Linking virtual gate to $V_{\mathrm{DS\_SAT}}$ vs. InAlAs doping

From the discussions on BAVETs changing in their doping from i- to p-type, through p-i-doping, V_{KNEE} is identified to be impacted by the presence of virtual gate. Reduction in $V_{\mathrm{DS\_SAT}}$ or V_{KNEE} occurs in the above mentioned order of doping type and the reduction occurs primarily through the changes in $V_{\mathrm{TH,DRAIN}}$. A virtual gate is associated with its own electrostatic potential (referred to as Ψ) which adjusts $V_{\mathrm{TH,DRAIN}}$ to anomalous values. The virtual gate has been suggested to reside at the drain-edge of the channel comprised in the region containing CBL/Aperture interface. Whether virtual gate originates from the traps at WBI needs to be studied further. However, it is clear that the Ψ_{VG}, $V_{\mathrm{TH,DRAIN}}$, V_{KNEE} are a strong function of the doping in InAlAs and change in an orderly manner for the doping designs chosen herein. We can further state that doping in InAlAs has a certain relationship to the electronic properties exhibited by the drain-edge of InGaAs channel. There are questions pertaining to the theory of virtual gate, which need further investigation. Information is needed on the location and distribution of virtual gate in L_{GO} and L_{AP} regions, isolating the energies in the bandgap that map to the Ψ_{VG} exhibited in each of the BAVET. Ongoing studies on $V_{\mathrm{DS\_SAT}}$ vs. field-plate, V_{GS}, and aperture width may provide more information on the modeling of BAVETs with a virtual gate.

4.10 Conclusion

It had been experimentally demonstrated that the use of p-doped region in the gate-barrier was beneficial in obtaining near-ideal $V_{\mathrm{DS\_SAT}}$ in BAVETs. $V_{\mathrm{DS\_SAT}}$ was studied by breaking it into two parts, namely in $V_{\mathrm{DS\_ON}}$, and the product of R_{ON} and $I_{\mathrm{D\_MAX}}$. Between these two primary constituents of $V_{\mathrm{DS\_ON}}$ was shown to have little bearing on $V_{\mathrm{DS\_SAT}}$ being both high and depending on doping in InAlAs. R_{ON} and $I_{\mathrm{D\_MAX}}$, and their

relationship to threshold voltage, primarily contributed to $V_{\mathrm{DS\_SAT}}$.

By comparison of R_{ON} and $I_{\mathrm{D\_MAX}}$ in i- and p-i-BAVETs, it was proposed that R_{ON} and $I_{\mathrm{D\_MAX}}$ can be decoupled due to the unequality expressed in threshold voltages at the source and drain edges of the channel, respectively. On the basis of the argument, it was stated that $V_{\mathrm{TH,DRAIN}}$ when anomalously high leads to high $V_{\mathrm{DS\_SAT}}$.

With regards to what causes the $V_{\mathrm{TH,DRAIN}}$ to behave in this manner, the theories of both impact ionization and a buried virtual gate were reasoned with. Experimental data suggested absence of impact ionization under the on-state conditions that exhibited high $V_{\mathrm{DS\_SAT}}$. High $V_{\mathrm{TH,DRAIN}}$ was proposed to be resulting due to a virtual gate, which is buried near the CBL/Aperture edge of channel, with its own electrostatic potential. This virtual gate response was weakened and its potential changed as the doping changes in the order of i-, p-i and p-type in the InAlAs layer of the gate-barrier and thus, the observed reduction in $V_{\mathrm{DS\_SAT}}$.

The results of varying the doping in gate-barrier were shown to be of fundamental significance since they gave an insight into the electronic properties of a region that is localized near the drain edge of the channel in BAVETs. The study made progress in addressing the following aspects of $V_{\mathrm{DS\_SAT}}$ in BAVETs: (a) a methodology to reduce $V_{\mathrm{DS\_SAT}}$ (b) an understanding on the mechanism controlling its behavior.

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Chapter 5

Aperture-based Field plating

5.1 Introduction

A high mobility material, like InGaAs, for channel is ideal to make a transistor with high frequency [1]. However, the low band gap limits the use of InGaAs in applications requiring high voltage operation [2]. In such case, a high band gap semiconductor, like that from the III-Nitride family, is an adequate replacement for InGaAs. This methodology is not without trade-offs, what is on one hand gained in bandgap is on the other hand lost in mobility [3].

There is another way to design a high frequency power transistor. An InGaAs-based transistor can be improved in its breakdown by a technique of wafer bonding [4, **?**]. A second material, like GaN, that has the property of containing high critical fields can be wafer-bonded to InGaAs to form the drift region of the device. High frequency and power have been so proposed to be obtainable in a transistor called wafer-bonded aperture vertical electron transistor, BAVET [6].

An earlier work investigated BAVETs for their off-state breakdown and pinch-off [5]. Impact-ionization was found to reduce breakdown in transistor and weaken its ability

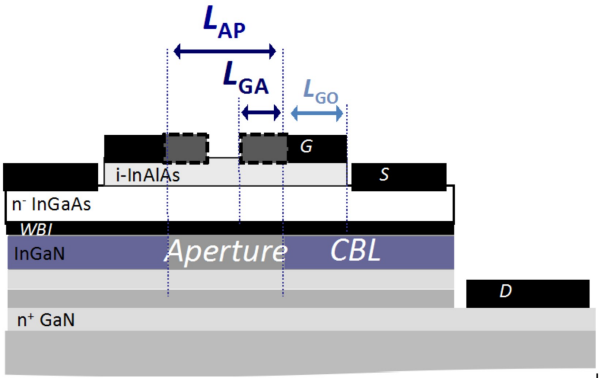


Figure 5.1: A cross sectional schematic of a BAVET in which its L_{GA}, L_{GO} and L_{AP} dimensions are defined. L_{GO} defines the region where channel overlaps with CBL and is modulated by gate. Gate is extended to overlap with the aperture over a dimension defined by L_{GA}. L_{AP} is the length of aperture. G, S, D represent gate, source and drain electrodes of BAVET. WBI represents the wafer-bonded interface that extends over aperture and CBL regions of channel.

to switch off. Extending the gate to overlap with aperture (shown as dimension L_{GA} in Fig. 5.1) benefitted in reducing impact-ionization.

The following questions, however, remained unexplained. a) What mechanism furnishes the field-plate effect in L_{GA}? b) If it is a low critical field or high peak field that leads to breakdown in BAVETs? c) Whether impact-ionization and field plating are characteristic to channel-current-blocking layer (CBL) or channel-aperture regions. A wafer-bonded interface (WBI) is additionally comprised in either region (see Fig. 5.1).

The problem of low breakdown is shown herein to be a result of both an unfavorably high electrostatic field that is sustained near the drain edge (ξ_{CBL}) and a low limit of critical electrostatic field to impact-ionization (ξ_{CRIT_IMPCT}).

It is also reported that in addition to L_{GA}, aperture length (L_{AP}) also affects the pinch-off in channel. These dimensions can be used to modify both lateral and vertical electrostatic field distributions in the vicinity of aperture and therefore control impact ionization and pinch-off.

Furthermore, how well a BAVET pinches-off is subject to two properties. One is

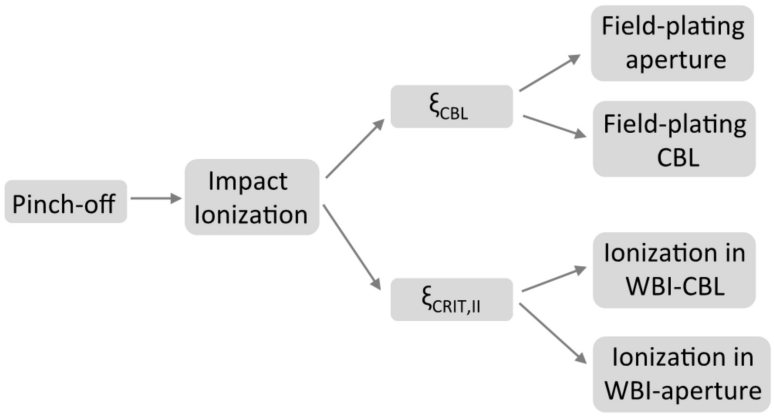


Figure 5.2: A flow chart is shown to depict the process of understanding impact-ionization, its mechanism and physical origin. ξ_{CBL} is the peak field and $\xi_{\mathrm{CRIT,II}}$is the field to impact-ionization, both of which are defined for the drain or CBL edge of a BAVET. ξ_{CBL} determines the nature of field-plating whereas $\xi_{\mathrm{CRIT,II}}$ establishes the limiting field beyond which impact-ionization is initiated. Impact-ionization depends on the relative behavior of the two fields.

the ability to field plate the aperture. The other depends on the critical field to impact ionization of CBL. The study defines a methodology to isolate the two phenomena. A flow chart of the investigation is constructed and shown in see Fig. 5.2.

The study proposes that the necessity of field plating to strong pinch-off implies that the device has a low critical field to impact ionization. Pinch-off is weakest for a device without an aperture, which highlights a second fact that instead of the channel-aperture, it is the channel-CBL region that impact ionizes.

5.2 Impact-Ionization

5.2.1 Condition to Impact Ionization

In a field-effect transistor (FET), gate-drain region of channel sustains the peak electrostatic field [7]. How high of an electrostatic field (ξ_{GD}) is sustainable in the gate-drain region, without initiating impact ionization, depends on a material property of the region,

which is its critical field to impact ionization ($\xi_{\text{CRIT\_IMPCT}}$). Onset of impact-ionization is eliminated if the following relation holds:

$$\xi_{\text{GD}} \ll \xi_{\text{CRIT\_IMPCT}} \tag{5.1}$$

In context of a BAVET, the gate-drain edge of the channel is the aperture-CBL edge of the device. The ξ_{GD} for a BAVET is hereinafter referred to as ξ_{CBL}. Experiments are designed to differentiate behavior of the two electrostatic fields.

5.2.2 Critical & Peak electric field in a BAVET

It is known from ref. [5] that impact-ionization related breakdown can weaken pinch-off in BAVETs. In such an event, ξ_{CBL} must exceed $\xi_{\text{CRIT\_IMPCT}}$ by means of a low $\xi_{\text{CRIT\_IMPCT}}$, and/or a high ξ_{CBL}. Therefore, impact-ionization-related breakdown can be regulated by either reducing ξ_{CBL} for a given $\xi_{\text{CRIT\_IMPCT}}$ or by raising latter for a given ξ_{CBL}.

$\xi_{\text{CRIT\_IMPCT}}$ of a device is known to be property of the material and is independent of lithographically-defined device dimensions [8]. Whereas $\xi_{\text{GD}}$of a FET is modifiable by the dimensions that determine field plating of the gate-drain region [9]. Likewise in a BAVET, the dependence of pinch-off on, for instance, L_{GA} dimension is likely a result of a change in ξ_{CBL} and not $\xi_{\text{CRIT\_IMPCT}}$. The following section states a method to reducing ξ_{CBL}.

5.2.3 L_{GA}, and L_{AP}-based Field plating to reduce ξ_{CBL}

In a FET, the extension of the gate towards the drain electrode serves the function of a gate-connected field plate. It modulates the depletion region of the gate-drain region and redistributes the electrostatic field such that a reduction in ξ_{GD} is obtained [9].

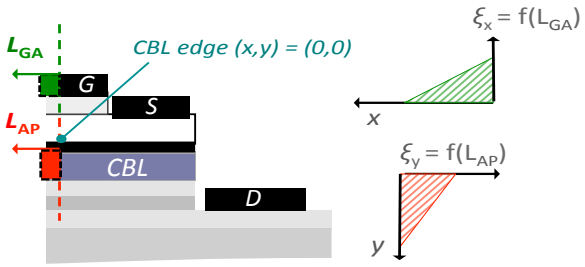


Figure 5.3: A half cross sectional schematic of BAVET is shown. Extending gate along L_{GA} and adding an aperture of dimension L_{AP} change lateral and vertical field distribution near the CBL edge. Lateral and vertical field profiles are shown as ξ_{X} vs. x and ξ_Y vs. y. For a given voltage, increase in L_{GA} extends field along L_{GA} and reduces the ξ_{CBL} at CBL edge. A similar change occurs in vertical field distribution by adding an aperture and so reduces ξ_{CBL}.

Another field-plating approach uses gate-drain separation length to reshape the electrostatics [10]. Similar principle of field plating is invoked herein to reduce impact-ionization through a reduction ξ_{CBL} but it is done so by means of L_{GA} and L_{AP} dimensions. If the electrostatic field distribution of aperture is modifiable by L_{GA} and L_{AP} then ξ_{CBL} may well be modified.

In the functioning of a BAVET, aperture absorbs a part of the drain voltage. In placing an aperture in the device, it allows electrostatic field to be distributed in the vertical direction (see Fig. 5.3). Therefore, L_{AP} can be modified to affect the pinch-off. For a given applied drain voltage the presence of an aperture (a non-zero L_{AP}), in contrast to its absence (L_{AP} of zero), may yield a lower ξ_{CBL}. Extending the gate laterally over the aperture, on the other hand, reshapes the field in the lateral direction (see Fig. 5.3). It is likely that increasing L_{GA} can reduce ξ_{CBL}. Experiments are conducted that investigate devices different in L_{AP} and L_{GA}.

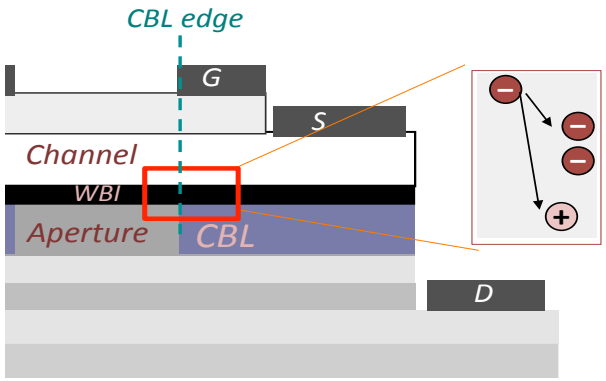


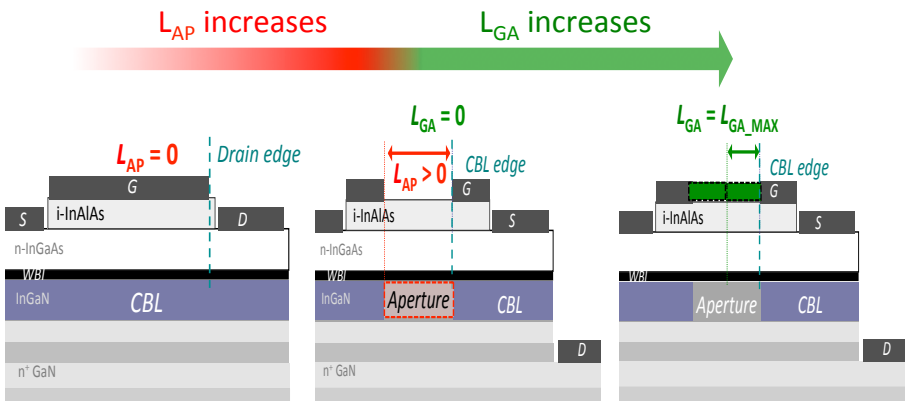
Figure 5.4: A partial cross sectional schematic of a BAVET wherein the regions in the vicinity of drain or CBL edge are highlighted using a box. The CBL edge comprises channel-WBI-CBL and channel-WBI-aperture regions. Weak pinch-off can arise due to impact-ionization of low $\xi_{\text{CRIT\_IMPCT}}$ of either CBL or aperture regions.

5.2.4 Using L_{AP} to understand $\xi_{\text{CRIT\_IMPCT}}$

Studying pinch-off vs. L_{AP} serves a two-fold purpose. (a) It identifies if $\xi_{\text{CRIT\_IMPCT}}$ is low or high by testing whether pinch-off is weak or strong, respectively in a device without a field-plate. (b) In removing aperture or field plate from a device, a case of L_{AP} set to zero; the channel is entirely placed on CBL. If channel-CBL region impact-ionizes and is what limits $\xi_{\text{CRIT\_IMPCT}}$ then a device without an aperture is expected to exhibit weak pinch-off. If however channel-aperture region impact-ionizes then the pinch-off is likely to improve by a reduction in L_{AP}. The study thus aids in finding the region of channel which impact ionizes (see Fig. 5.4). In other words, information on $\xi_{\text{CRIT\_IMPCT}}$ of channel WBI-aperture and WBI-CBL regions may be revealed.

5.3 Experiment & Measurement Method

The experiment comprises of fabricating devices with different L_{GA} and L_{AP}(see Fig. 5.5). Devices comprise of an InAlAs gate barrier that is doped unintentionally (referred to as i-InAlAs in Fig. 5.5).



(a) (b) (c)

Figure 5.5: Three types of devices, which differ in their L_{AP} and L_{GA}, are fabricated for this study. (a) A schematic of a device without an aperture. It is a later HFET biased with a drain contact to InGaAs. L_{AP} changes from 0 to greater than zero between (a) and (b). (b) A schematic of a BAVET is shown which comprises of an aperture and an L_{GA} set to zero. Between (b) and (c), L_{GA} is incrementally changed. (c) A schematic of a BAVET with an L_{GA} of $L_{\mathrm{GA\_MAX}}$. Dashed lines marks the drain edge of HFET in (a) and CBL edge of BAVETs in (b) and (c). These devices comprise an unintentionally doped InAlAs.

5.3.1 Choice of L_{GA} and L_{AP} dimensions and their Design

With regards to investigating pinch-off in response to the presence of an aperture, devices with two types L_{AP} are considered. It is either equal to or greater than zero and are referred to as $L_{\mathrm{AP=0}}$ and $L_{\mathrm{AP>0}}$, respectively (see Fig. 5.5(a) and (b)). Aperture regions are defined during the ion-implantation step to form CBL [11]. In a device with $L_{\mathrm{AP=0}}$, the channel is placed over a region that is entirely in CBL (see Fig. 5.5(a)). $L_{\mathrm{AP>0}}$, on the contrary, adds an aperture such that one part of the channel overlaps with the aperture and another part with CBL (see Fig. 5.5(b)). By changing the L_{AP} in this way, the device topology is changed from lateral to vertical. Specifically, a device with $L_{\mathrm{AP>0}}$ can be treated and characterized as a heterojunction FET (HFET), a lateral transistor (see Fig. 5.5(a)). A BAVET is however represented by a device with $L_{\mathrm{AP>0}}$ (see Fig. 5.5(b)).

BAVETs are fabricated with an L_{GA} that is either L_{GA_MAX}, which is half of L_{AP}, or zero (see Fig. 5.5(a) and (b)). The latter is hereinafter referred to as $L_{GA=0}$. Fabrication of such devices is described in ref. [5]. A device with $L_{GA=0}$ is also the device with $L_{AP>0}$ (see Fig. 5.5(b)).

The bias conditions change between BAVET and HFET in that one of the source electrodes to InGaAs in former is a drain electrode in latter (see Fig. 5.5(a) and (b)). The breakdown of a lateral transistor is characterized against a vertical transistor in a comparison of pinch-off between HFET and BAVET.

5.3.2 Characterization of Pinch-off by Threshold Voltage

The quality of pinch-off can be estimated from I-V_{GS} measurements [7]. It is used to estimate how much of a gate voltage, referred to as threshold voltage (V_{TH}), is needed to pinch-off the current. Any degree of change in V_{TH} therefore marks the change in pinch-off. For instance, an anomalous reduction in V_{TH} from one device to another may be an evidence of weakening of pinch-off.

Herein, V_{TH} is extracted from the trace of source-current (I_S) vs. gate-source voltage (V_{GS}). Pinch-off represents the condition of $I_S = 0$. I_S-V_{GS} trace for a given V_{DS} is linearly fitted as shown in Fig. 5.6. In devices, which are unable to pinch-off in the permissible voltage range, the threshold voltage is extracted from the x-axis intercept of a linear fit to I_S-V_{GS} trace. Fig. 5.6 shows the method of extraction. I_S-V_{GS} measurements shown herein comprise of two regimes of V_{GS}. The regimes are determined by two x-axis intercepts, V_{TH_1} and V_{TH_2} in Fig. 5.6. It is yet to be understood on why the two-regime characteristic but it is found to be generally present in the devices under investigation.

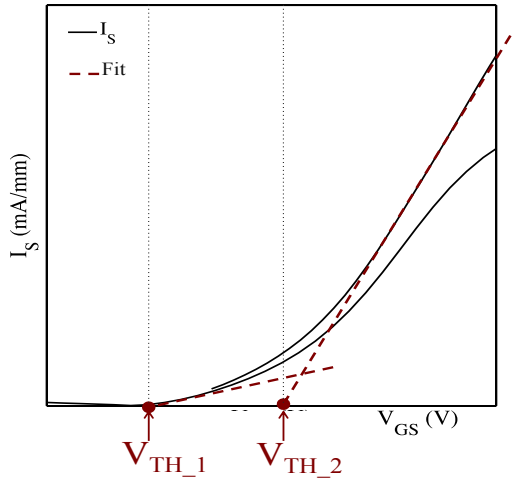


Figure 5.6: I_{D}-V_{GS} characteristics of a BAVET measured for two V_{DS}. The experimentally measured trace is shown by a solid line, which is linearly fitted. The fitted traces are plotted in dashed-line form. $V_{\mathrm{TH\_1}}$, and $V_{\mathrm{TH\_2}}$ are x-intercepts for lines fitted in nearly on and nearly off regimes. I-V_{GS} comprises of two regimes defined by $V_{\mathrm{TH\_1}}$ and $V_{\mathrm{TH\_2}}$. $V_{\mathrm{TH\_1}}$ is an extrapolated valued derived from the linear fit that is extended to $I_{\mathrm{S}} = 0$ mA.mm^{-1}.

5.4 Results: Pinch-off vs. L_{GA} And L_{AP}

I_{S}-V_{GS} is measured for three different types of devices and corresponding V_{TH} is extracted. It is found that $V_{\mathrm{TH\_1}}$ (a) changes significantly in comparison to $V_{\mathrm{TH\_2}}$ among the three devices, and (b) primarily determines the threshold voltage and pinch-off of a device. The study therefore focuses on $V_{\mathrm{TH\_1}}$ and hereinafter, adopts it as V_{TH} of a device. Within the scope of this work, the terms such as weaker pinch-off, lower breakdown, and higher impact ionization may be treated as equivalent to a lower or more negative V_{TH}.

5.4.1 I_{S}-V_{GS} vs. L_{AP}

For V_{TH} vs. L_{AP}, a BAVET with $L_{\mathrm{AP}>0}$, and an i-HFET are compared. The devices differing in L_{AP} are found to differ in their V_{TH}. Absence of pinch-off is a common characteristic in the two devices but V_{TH} is more negative and pinch-off is weakest for that with $L_{\mathrm{AP}=0}$ (Fig. 5.7(a) and (b)).

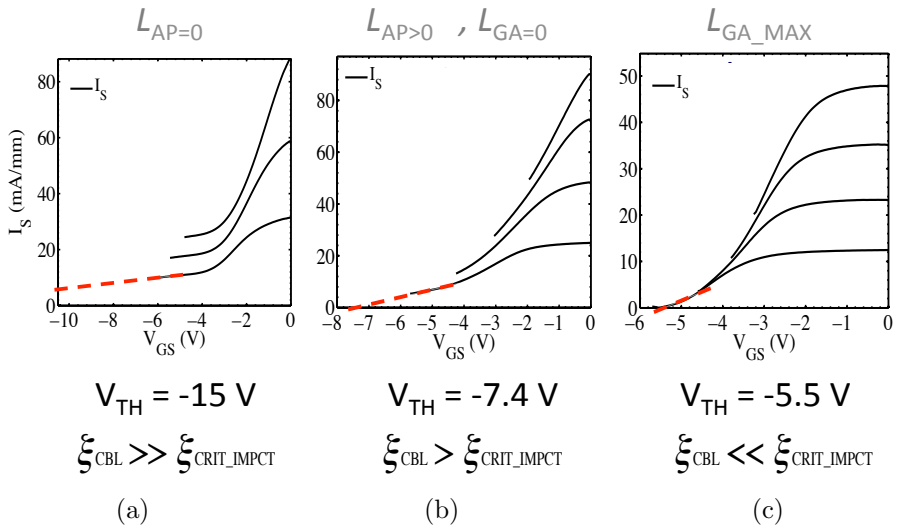


Figure 5.7: I_D-V_{GS} measurements are shown for (a) HFET with $L_{AP} = 0$, (b) BAVET with $L_{AP} > 0$ and L_{GA}= 0 and (c) a BAVET with L_{GA}= L_{GA_MAX}. For (b) and (c) and L_{AP} of 8 μm is employed. V_{DS} varies between 2 to 4 V in steps of 1 V for (a), whereas it is varied form 4 to 10 V in steps of 2 V. A dashed line in each curve shows the linear fit to extract V_{TH} of the device. As pinch-off gets stronger, V_{TH} becomes less negative from (a) to (c). Each device sustains a different ξ_{CBL}, which is evident from the equation comparing ξ_{CBL} and ξ_{CRIT_IMPCT}.

5.4.2 I_S-V_{GS} vs. L_{GA}

Fig. 5.7(b) and (c) present the I_S-V_{GS} traces of i-BAVETs with $L_{GA=0}$ and L_{GA_MAX}, respectively. Pinch-off is obtained for the latter at a V_{TH} of -5.51 V. For a device with $L_{GA=0}$, pinch-off is weak, which on linear fitting reveals a V_{TH} of -7.4 V. It is deduced that reducing L_{GA} reduces the ability of transistor to pinch-off.

5.4.3 V_{TH} vs. L_{AP} and L_{GA}

Both L_{GA} and L_{AP} correlate to aperture electrostatics either indirectly through gate or directly in the size of aperture. Therefore, V_{TH} can be plotted against a combined set of aperture-related dimensions that change from L_{GA_MAX} to $L_{AP=0}$ through $L_{GA=0}$ or $L_{AP>0}$. Such a representation is shown in Fig. 5.8.

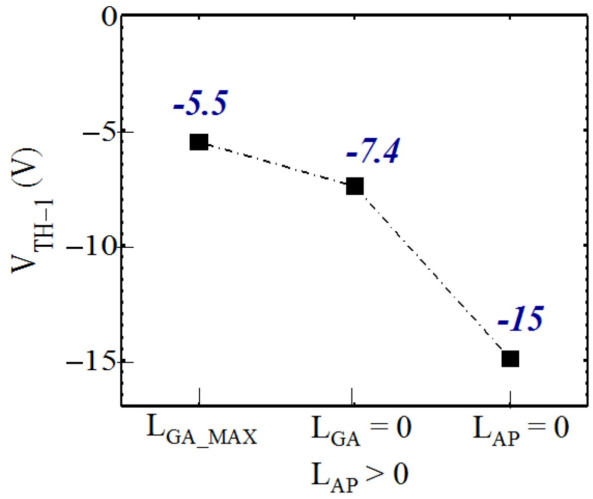


Figure 5.8: $V_{\mathrm{TH\_1}}$ is plotted against aperture-related dimensions of L_{GA} and L_{AP}. $V_{\mathrm{TH\_1}}$ becomes anomalously more negative for a reduction in either L_{GA} or L_{AP}.

An interesting trend is evident in Fig. 5.8 and can be summarized in a statement that V_{TH} reduces in the manner that a maximum pinch-off is available in $L_{\mathrm{GA\_MAX}}$ and minimum in $L_{\mathrm{AP=0}}$. V_{TH} and pinch-off reduces with L_{GA} and L_{AP} (see Fig. 5.8).

5.5 Discussion

This section provides an explanation of the above mentioned results and addresses the following questions. (a) If it is drain-induced barrier lowering (DIBL) or gate-leakage or impact-ionization that prevents pinch-off in devices with $L_{\mathrm{AP=0}}$ and $L_{\mathrm{GA=0}}$ (see Fig. 5.7(a) and (b))? (b) What mechanism makes V_{TH} dependent on L_{GA} and L_{AP} in Fig. 5.8? (c) What information pertaining to ξ_{CBL} and $\xi_{\mathrm{CRIT\_IMPCT}}$ can be derived? (d) Does the analysis pinpoint the region, which primarily limits pinch-off in a BAVET?

5.5.1 Impact-ionization in a device with $L_{\mathrm{GA=0}}$

V_{TH} close to -5.5 V is what is expected based on the doping and thicknesses of InAlAs and InGaAs. However, neither $L_{\mathrm{AP=0}}$ nor $L_{\mathrm{GA=0}}$, but $L_{\mathrm{GA\_MAX}}$, meet the expectation in

V_{TH}, in spite of being similar in their gate-barrier and channel.

A prior work eliminated DIBL and gate-leakage as the possible causes of weak pinch-off in a device with $L_{GA=0}$ [5]. It was additionally proposed that the device suffered in pinch-off due to impact ionization in the CBL edge of the device.

5.5.2 Impact-ionization in a device with $L_{AP=0}$

Weak pinch-off adversely affects a device without an aperture, an HFET. An increase in gate length and lowering of gate leakage is found to be ineffective to improving pinch-off. The cause of which is so ascertained to be impact-ionization related breakdown near the drain edge. The following section answers the questions on why the removal of L_{GA} or L_{AP} leads to anomalously low V_{TH} and why such dependence?

5.5.3 Field-plating to reduce ξ_{CBL} and impact-ionization

A similar impact-ionization-related breakdown occurs at the drain edge of an HFET and a BAVET with $L_{GA=0}$. Let us next reason on the observed reduction in V_{TH} on reducing L_{GA} and L_{AP}, as shown in Fig. 5.8. As was proposed in an earlier section, an increase in L_{AP} or L_{GA} reduces ξ_{CBL} by reshaping the lateral and vertical field distribution. Experimental results show pinch-off improves or impact-ionization reduces as L_{AP} and L_{GA} are increased. The presence or absence of impact-ionization is a clear function of aperture electrostatics, primarily ξ_{CBL}, in a BAVET (see Fig. 5.7). The mechanism correlating V_{TH} to aperture-related dimensions is hence found for a BAVET.

Using L_{GA_MAX} yields lowest ξ_{CBL} in comparison to $L_{GA=0}$ and $L_{AP=0}$ (see Fig. 5.7). L_{GA_MAX} plays a role in field plating the device. Conversely, it is argued that in making L_{GA} or L_{AP} go to zero, field plating is reduced and pinch-off is weakened.

5.5.4 $\xi_{\text{CRIT\_IMPCT}}$ and its relation to channel-WBI-CBL region

A BAVET needs field plating to reduce ξ_{CBL} in order to achieve pinch-off in channel (see Fig. 5.8). For this reason we are led to believe that the devices are generally low in their $\xi_{\text{CRIT\_IMPCT}}$. $L_{\text{GA\_MAX}}$ sustains ξ_{CBL} as low as that which meets the condition of (5.1).

The weakest pinch-off is observed for an HFET, which has no aperture (see Fig. 5.7(a) and 9). The device has its peak field at the drain edge, which comprises WBI-CBL regions of channel. In other words, weak pinch-off is a characteristic of WBI-CBL region at the drain end of the device (see Fig. 5.9). The region-containing aperture does not impact-ionize in comparison to that of CBL (see Fig. 5.4). Aperture region is merely a means to effect field plating.

A low $\xi_{\text{CRIT\_IMPCT}}$ combined with the fact that impact-ionization is local to WBI-CBL region of channel implies that it is this region which exhibits a low $\xi_{\text{CRIT\_IMPCT}}$. Channel-WBI-CBL region thus pose a limiting condition to breakdown of BAVETs. Increasing $\xi_{\text{CRIT\_IMPCT}}$ to mitigate impact-ionization will be addressed in another study. However, herein the method of employing L_{GA} of $L_{\text{GA\_MAX}}$, reduces ξ_{CBL} to a value less than $\xi_{\text{CRIT\_IMPCT}}$, and gains an improved pinch-off behavior.

5.6 Conclusion

Impact-ionization that was found in BAVETs by S. Lal et al in [5]was further investigated. Its cause, control mechanism, and relationship to device features were identified and formulated. The facts of impact ionization and field plating were used to explain the theory of off-state response in BAVETs.

This work proved that a change of pinch-off through device dimensions is a result of a change in ξ_{CBL} and not $\xi_{\text{CRIT\_IMPCT}}$. Employing an L_{GA} of $L_{\text{GA\_MAX}}$ is effective to re-

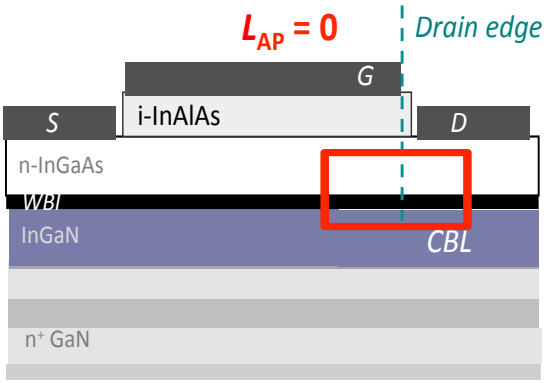


Figure 5.9: A cross sectional schematic is shown for a device without an aperture. Channel is disposed on CBL regions. A dashed line marks drain edge of the device. The drain edge resides in channel-WBI-CBL region. A weak pinch-off in a device is due to impact-ionization in CBL region of channel.

ducing ξ_{CBL}, mitigating impact-ionization and so improving pinch-off. $L_{\mathrm{GA\_MAX}}$ provides the functionality of a field plate by reshaping the lateral and vertical field distributions. In studying dependence of pinch-off on L_{GA} and L_{AP}, a method to modify ξ_{CBL} for a given ξ_{CRIT_IMPACT} is furnished.

Results also made evident the physical origin of impact-ionization in the device. The channel-WBI-CBL region primarily limits ξ_{CRIT_IMPACT} of the device. The need for modifying ξ_{CBL} to values lower than ξ_{CRIT_IMPACT} was shown to be an essential condition. A condition met by increasing L_{GA} and L_{AP}. The nature of channel-WBI in aperture and CBL regions were found to determine ξ_{CBL} and $\xi_{\mathrm{CRIT\_IMPCT}}$, respectively.

The work succeeded in understanding and resolving the problem of breakdown in BAVETs by means of field-plating the aperture. Additionally, information is revealed on how WBI-CBL region of the channel determines the property of critical field to impact ionization.

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Chapter 6

Enhancing Critical Field to Impact Ionization

6.1 Introduction

Wafer-bonded vertical transistors, BAVETs, were shown to improve in pinch-off by a method of field plating [1]. Interesting information was additionally revealed on off-state breakdown mechanism in BAVETs. Firstly, field plating of channel-aperture reduces peak field (ξ_{CBL}) in channel-CBL region. Secondly, the work revealed that devices suffer with a low critical field to impact ionization ($\xi_{\mathrm{CRIT\_IMPCT}}$), a property found to be local to channel-CBL region. In the event of a low $\xi_{\mathrm{CRIT\_IMPCT}}$, adding field plate is essential to obtaining a strong off-state pinch-off.

This work extends the study on pinch-off but focuses on understanding $\xi_{\mathrm{CRIT\_IMPCT}}$ and explores on following questions. What property of channel-CBL region regulates $\xi_{\mathrm{CRIT\_IMPCT}}$, whether it is the channel or wafer-bonded interface (WBI) between channel and CBL that impact ionizes (see Fig. 6.1)? Can $\xi_{\mathrm{CRIT\_IMPCT}}$, a material property, of a BAVET be enhanced to eliminate impact ionization, without the recourse of adding a

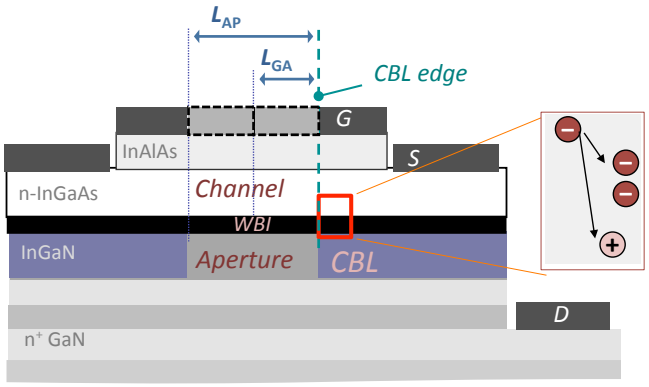


Figure 6.1: A cross sectional schematic of a BAVET is shown. Impact-ionization phenomenon occurs in the boxed region, which comprises channel, wafer-bonded interface (WBI) and current-blocking layer (CBL) region. L_{GA} and L_{AP} dimensions are used to influence the peak field at drain or CBL edge.

field plate?

Herein, experiments are conducted that fabricate devices varying in length of aperture (L_{AP}) and gate-aperture overlap (L_{GA}) (see Fig. 6.1). Extraction of their threshold voltage (V_{TH}) and pinch-off serves the purpose of isolating field-plate effect and behavior of ξ_{CBL}. Two dimensions are together referred to as aperture-related dimensions. A second experiment aimed at understanding ξ_{CRIT_IMPCT} studies V_{TH} vs. L_{GA} and L_{AP} in two types of devices, one wherein p-doped InAlAs is used while in the other it is doped unintentionally. The former is referred to as a p-BAVET and latter as an i-BAVET. Different mechanisms that are investigated in this work are summarized in a flow chart shown in Fig. 6.2.

Results indicate that pinch-off is successfully obtained in a p-BAVET and that it is so achieved in the absence of a field-plate effect. A fact that implies, on one hand, an absence of impact-ionization and on the other, a possibility that device exhibits a higher ξ_{CRIT_IMPCT}. A comparison of V_{TH} between i- and p-BAVETs proves that ξ_{CRIT_IMPCT} is enhanced in the latter.

The work presents a method to obtain high critical field in such devices. It further

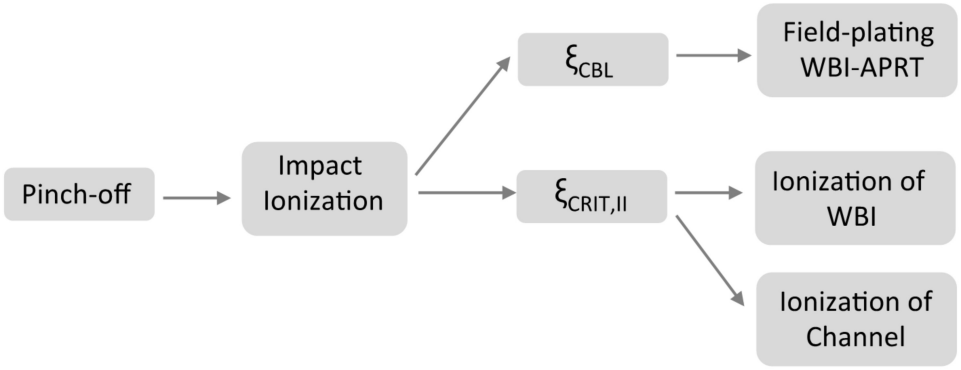


Figure 6.2: The study follows a process of investigation shown in the form of a flow chart. Relationship of pinch-off and impact ionization with ξ_{CBL} and $\xi_{CRIT_IMPCT}$is first isolated. The study also finds if $\xi_{\mathrm{CRIT\_IMPCT}}$ is a property determined by channel or WBI.

proposes that a change in the impact ionization behavior of WBI yields the favorable change in material property of $\xi_{\mathrm{CRIT\_IMPCT}}$ in a BAVET.

6.2 Impact-Ionization

6.2.1 Critical and Peak electric field in a BAVET

The following theory regarding breakdown in BAVETs is recalled from ref. [1]. A $\xi_{\mathrm{CRIT\_IMPCT}}$ that is greater than ξ_{CBL} is what eliminates impact-ionization in a BAVET. A condition represented by equation:

$$\xi_{\mathrm{CBL}} \ll \xi_{\mathrm{CRIT\_IMPCT}} \tag{6.1}$$

Maintaining (6.1) eliminates impact-ionization related adverse influence on V_{TH}, pinch-off and breakdown of a transistor. Field plating for low ξ_{CBL} works to the purpose, but it is desirable that a BAVET achieve improved off-state performance from a property of a high $\xi_{\mathrm{CRIT\_IMPCT}}$.

6.2.2 Pinch-off behavior for low or high ξ_{CBL} and $\xi_{\mathrm{CRIT\_IMPCT}}$

With L_{GA} and L_{AP} effecting aperture's electrostatics, pinch-off or V_{TH} vs. L_{GA} and L_{AP} may gain us information on how high ξ_{CBL} can get and how high of a $\xi_{\mathrm{CRIT\_IMPCT}}$ is available from the device.

It is also true that while ξ_{CBL} is a property of device that is associated with dimensions like L_{GA} and L_{AP}, $\xi_{\mathrm{CRIT\_IMPCT}}$ being a material property is, however, likely to remain unchanged for any change in such dimensions. There can be two scenarios, one wherein L_{GA} and L_{AP} strongly influence V_{TH}, and the other where it is independent of L_{GA}, or L_{AP}.

If V_{TH} is a function of L_{GA} and L_{AP}, it implies that ξ_{CBL} is changed for a constant $\xi_{\mathrm{CRIT\_IMPCT}}$. And additionally, if pinch-off is weak then it may be a case of a high ξ_{CBL} in a region of low $\xi_{\mathrm{CRIT\_IMPCT}}$. Pinch-off becomes more sensitive to changes in ξ_{CBL} especially if $\xi_{\mathrm{CRIT\_IMPCT}}$ is low.

A second scenario may also exist. ξ_{CBL} is (a) high and (b) unaffected by field plating if devices exhibit strong pinch-off and if V_{TH} is unchanged with L_{GA} or L_{AP}, respectively. Conversely, a strong pinch-off, or absence of impact-ionization, in spite of high ξ_{CBL} can exist only if the material is associated with a high $\xi_{\mathrm{CRIT\_IMPCT}}$. Therefore, behavior of pinch-off and changes in V_{TH} with aperture dimensions are two factors that can effectively isolate the two conditions, namely (a) a low ξ_{CBL} and low $\xi_{\mathrm{CRIT\_IMPCT}}$, and (b) a high ξ_{CBL} and high $\xi_{\mathrm{CRIT\_IMPCT}}$. Case (b), if found, may act as a method to make $\xi_{\mathrm{CRIT\_IMPCT}}$ high.

An instance of case (a) was experimentally deduced in BAVETs of ref. [1]. A positive coefficient between V_{TH} and L_{GA} or L_{AP} led to a deduction that a device without a field plate sustains a high ξ_{CBL} for a low $\xi_{\mathrm{CRIT\_IMPCT}}$. These types of BAVETs, referred to as i-BAVETs, comprised unintentionally doped InAlAs. A similar test of pinch-off and

V_{TH} is performed herein but for another type of BAVETs, wherein the InAlAs is doped p-type.

In this work we seek if using p-doped InAlAs achieves a high $\xi_{\mathrm{CRIT\_IMPCT}}$ in a BAVET. If pinch-off is achieved and V_{TH} is found independent of the aperture-related dimensions, then it can be stated to be so because of a p-BAVET exhibiting a high $\xi_{\mathrm{CRIT\_IMPCT}}$.

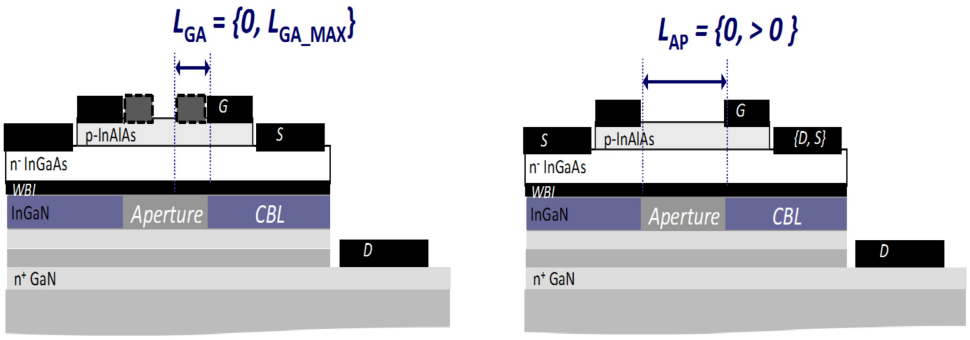
6.2.3 $\xi_{\mathrm{CRIT\_IMPCT}}$ a property of channel or WBI

$\xi_{\mathrm{CRIT\_IMPCT}}$ is a material property. The channel's band gap primarily determines $\xi_{\mathrm{CRIT\_IMPCT}}$ in a field effect transistor (FET) [2], [3]. In the case of a BAVET, a low $\xi_{\mathrm{CRIT\_IMPCT}}$ in CBL regions may originate in either its channel or WBI (see Fig. 6.1). Channel is comprised in InGaAs, a semiconductor known to be limited in its critical field [4]. While with regards to a WBI, information on its $\xi_{\mathrm{CRIT\_IMPCT}}$ is unavailable. Finding the physical origin of low $\xi_{\mathrm{CRIT\_IMPCT}}$ in a BAVET and advancing our knowledge on a WBI's $\xi_{\mathrm{CRIT\_IMPCT}}$ are two aspects that may be addressed in this study.

An experiment is conducted that clearly distinguishes between the two possible regions of impact ionization, namely channel and WBI. The principal of the experiment is that if a change of pinch-off through $\xi_{\mathrm{CRIT\_IMPCT}}$ happens without a change in bandgap of channel, then it is so due to a change in WBI and its property of $\xi_{\mathrm{CRIT\_IMPCT}}$. The experimentation may further find an answer on how to raise $\xi_{\mathrm{CRIT\_IMPCT}}$ of a WBI.

6.3 Experiment and Measurement Method

Three different sets of devices are fabricated for this study. Devices (a) differing in dimensions of L_{GA} and L_{AP}, (b) with and without InAlAs extended over the aperture region, and (c) comprising unintentional and p-doped InAlAs (see Fig. 6.3, 6.4, and 6.5). For (a) and (b), InAlAs is either doped p-type or unintentionally.



(a) (b)

Figure 6.3: Devices fabricated for an experiment to understand ξ_{CBL} in p-devices. (a) Schematic structure of a BAVET is shown with its L_{GA} dimension. Two devices are fabricated, one with an L_{GA} of 0 and other comprising $L_{\mathrm{GA\_MAX}}$, which is half of aperture length. Devices fabricating with different L_{AP} are shown in (b). An L_{AP} of zero results in an HFET while a BAVET is obtained if $L_{\mathrm{AP}} > 0$. The drain electrode contacts the channel for the former. The devices dimensions are similarly modified for those with unintentionally doped InAlAs, referred to as i-devices.

6.3.1 Variations in L_{GA} and L_{AP}

L_{GA} and L_{AP} were found to influence ξ_{CBL} in i-BAVETs through field plating effect [1]. The study is repeated herein but with a goal of exploring if similar field plating occurs in p-BAVETs. L_{GA} is chosen to be either zero or $L_{\mathrm{GA\_MAX}}$, whereas L_{AP} can be zero or greater than zero (see Fig. 6.3(a) and (b)). The devices are named as $L_{\mathrm{GA=0}}$, $L_{\mathrm{GA\_MAX}}$, $L_{\mathrm{AP=0}}$, $L_{\mathrm{AP>0}}$, respectively. A device with $L_{\mathrm{AP=0}}$ is a heterojunction field-effect transistor (HFET) comprising a drain electrode in contact with the InGaAs channel (see Fig. 6.3(b)). These dimensions are defined by lithography techniques and are detailed in [5] and [6].

6.3.2 Etching p-InAlAs over aperture

It can be argued that InAlAs in L_{AP} regions, with its p-doping, can provide an additional field-plate effect to the n-doped InGaAs channel through p-n junction electrostatics. Therefore, there is a possibility that the pinch-off may be changed in the presence

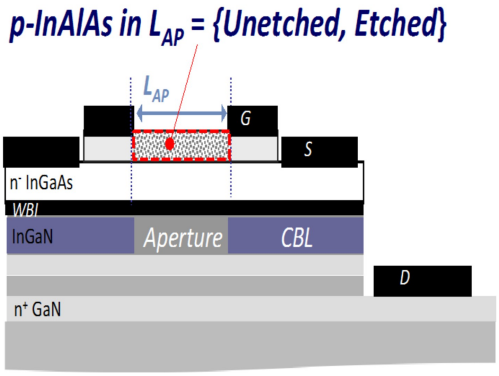


Figure 6.4: Two types of devices are fabricated which differ in their channel depletion from a p-doped InAlAs in L_{AP} regions. The difference is brought about by selectively etching InAlAs such that it is absent in L_{AP} regions but present under the gate electrode (marked by G). Two p-BAVETs are referred to as etched and unetched, wherein InAlAs is etched in the former while in the latter it is retained. and the other in which it is not. The devices are tested for any change in pinch-off and ξ_{CBL}.

or absence of p-InAlAs over aperture region of the channel such that pinch-off is made weaker in the latter. The argument is tested for in an experiment, wherein p-InAlAs is selectively etched over the L_{AP} region (see Fig. 6.4). A wet etch is performed for the purpose. Experiment so yields two devices, namely, unetched and etched p-BAVETs, wherein the former comprises p-InAlAs over aperture region while the latter is without it (see Fig. 6.4).

6.3.3 Choice of doping of InAlAs

A third experiment is conducted which changes doping in InAlAs and studies its impact on field plate effect and impact ionization. In one device, referred to i-device, InAlAs is doped unintentionally while in the other employs p-doped InAlAs and is referred to as p-device (see Fig. 6.5). A third variation to doping is also performed wherein InAlAs is doped p-type over a part of its thickness while it is doped unintentionally in the part that is placed next to InGaAs. Such a device is referred to as a p-i-BAVET.

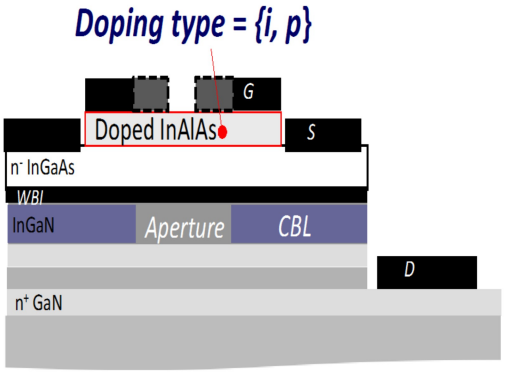


Figure 6.5: An experiment to deduce $\xi_{\text{CRIT\_IMPCT}}$ in BAVETs is conducted. The doping in InAlAs is varied between uniform p-doping or unintentional doping. Influence of L_{GA} and L_{AP} variations are studied for both p and i-BAVETs. A third variation is briefly discussed too wherein there are two parts of InAlAs one is p-doped while the other is unintentionally doped, and these devices are referred to as p-i-BAVETs.

6.3.4 Characterization of Critical and Peak fields through V_{TH}

A strong or weak pinch-off in source current (I_{S}) implies the presence or absence of impact ionization [1]. For instance, if a device with $L_{\text{AP=0}}$ is able pinch-off then it proves that impact-ionization is non-existent at the drain edge or its channel-WBI-CBL region (see Fig. 6.3(b) and 6.1).

The quality of pinch-off is additionally represented in threshold voltage (V_{TH}). A V_{TH} that is anomalously negative is an evidence of weak pinch-off. The method of extracting V_{TH} from the off-state regime of I_{S}-V_{GS} is shown in ref. [1].

ξ_{CBL} is herein interpreted in behavior of V_{TH} versus L_{GA}, and L_{AP}. Whereas, if V_{TH} vs. InAlAs doping is characterized under the condition that L_{GA} and L_{AP} dimensions are unchanged and so, ξ_{CBL}, then the changes in V_{TH} effectively represent the behavior of $\xi_{\text{CRIT\_IMPCT}}$ vs. InAlAs doping.

6.3.5 Method to isolate between channel and WBI as region that impact-ionizes

A line of thought is followed to find the feature limiting breakdown and pinch-off in BAVETs. If pinch-off is unchanged and weak between i- and p-BAVETs, then it is certain that their common feature of InGaAs channel is what impact ionizes. InGaAs is a material that lacks in breakdown on account of its lower $\xi_{\mathrm{CRIT\_IMPCT}}$ and bandgap of InGaAs channel [4]. If the pinch-off is, on the other hand, dramatically impacted by the doping in InAlAs, wherein the device goes from being unable to being able to pinch-off, then the results eliminate the channel impact-ionization but raise the possibility of ionization of WBI.

6.4 Results

6.4.1 I_S-V_{GS} and V_{TH} vs. L_{GA}, L_{AP} for p-BAVETs

A p-device exhibits strong pinch-off in I_S-V_{GS} measurements. This attribute is found to be generally present, in other words, pinch-off is obtained irrespective of choice of L_{GA}, L_{AP} or etched and unetched InAlAs. Fig. 6.6(a) shows the I_S-V_{GS} and pinch-off in one type of p-BAVET, with $L_{GA=0}$. The similarity in pinch-off is reflected in V_{TH}, which is nearly constant and independent of different L_{GA}, and L_{AP} in Fig. 6.6(b). Etching InAlAs over L_{AP} regions makes no difference to V_{TH} either.

6.4.2 I_S-V_{GS} and V_{TH} for i-BAVETs

We next characterize pinch-off and V_{TH} in i-devices. A weak pinch-off is present for a device with $L_{GA=0}$ or $L_{AP>0}$, making its V_{TH} anomalously negative (see Fig. 6.7).

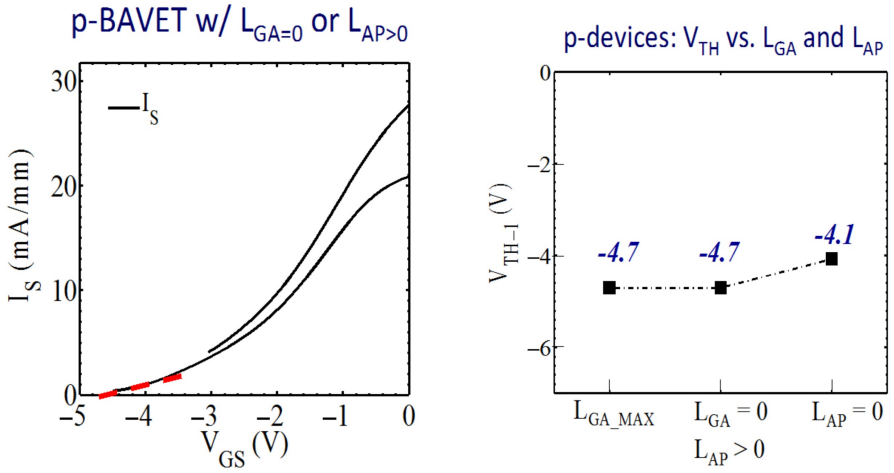


Figure 6.6: (a) I_{D}-V_{GS} of a p-BAVET with $L_{\mathrm{GA=0}}$ or $L_{\mathrm{AP>0}}$. V_{DS} varies from 4 to 6 V in steps of 2 V. A strong pinch-off is observed in I_{S}. A dashed line is linearly fitted to extract V_{TH}, which is -4.7 V. BAVETs whether with $L_{\mathrm{AP}} = 0$ or $L_{\mathrm{GA\_MAX}}$, or comprising etched or unetched InAlAs, are not shown herein but are found to be similar to (a) in pinch-off. (b) V_{TH} is traced different L_{GA} and L_{AP}. A strong and similar pinch-off implies impact-ionization is absent and that each device sustains a similar ξ_{CBL} for a given $\xi_{\mathrm{CRIT\_IMPCT}}$, respectively.

Fig. 6.7(b) shows that this anomaly is also present in the case of $L_{\mathrm{AP=0}}$ but is favorably eliminated if $L_{\mathrm{GA\_MAX}}$ is employed.

Comparison of Fig. 6.6 to 6.7 reveals that a p-device is dramatically better than an i-device in (a) how well it pinches-off, (b) how much less anomalous is its V_{TH}, and (c) its relationship to aperture-related dimensions.

6.4.3 V_{TH} vs. InAlAs doping

The distinct nature of pinch-off in i- and p-devices makes it necessary to trace V_{TH} as a function of doping in InAlAs. BAVETs with $L_{\mathrm{GA=0}}$ are chosen for the purpose. Fig. 6.8 shows box plot V_{TH} for p, p-i and i-BAVETs. Median V_{TH} is least anomalous for p-devices, whereas i- and p-i-devices suffer in V_{TH} such that their median is abnormally negative. Likewise, pinch-off is absent in i- and p-i-devices while p-devices are able to

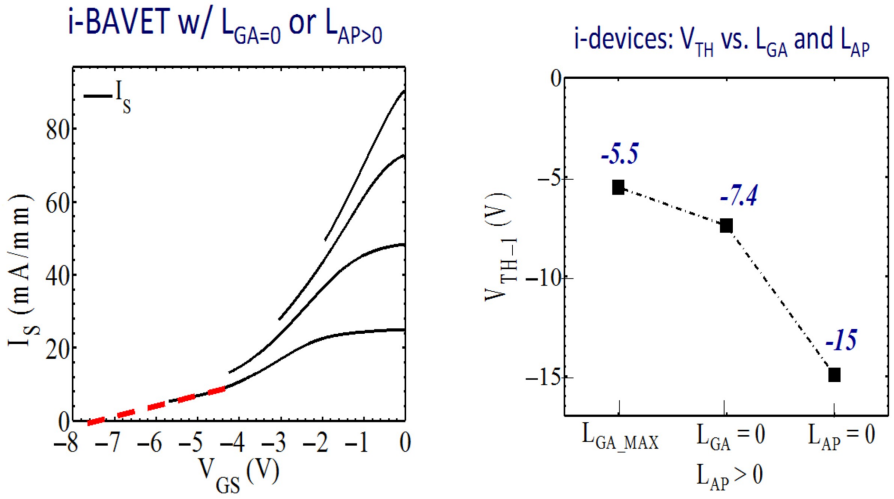


Figure 6.7: Weak pinch-off in i-devices is depicted in (a) I_S-V_{GS} characteristics of an i-BAVET with $L_{GA=0}$ and (b) V_{TH} vs. L_{GA}, L_{AP} trace. V_{TH} can be extrapolated extending the dashed line to x-axis. Absence of L_{GA} and L_{AP} are detrimental to V_{TH} in i-devices and unfavorably increase impact-ionization. V_{TH} of an HFET is most negative while that of L_{GA_MAX} is least. A weak and L_{GA}, L_{AP}-dependent pinch-off, firstly, implies that impact-ionization arises due to a low ξ_{CRIT_IMPCT} and secondly, that it is a function of L_{GA} and L_{AP} through ξ_{CBL}.

pinch-off. It is therefore deducible that the doping of InAlAs gate-barrier determines how well a BAVET pinches off.

6.5 Discussion: Critical Field And InAlAs Doping

A change in InAlAs doping changes built-in voltage (V_{BI}) of InAlAs-InGaAs junction, and so may influence V_{TH}. It is expected then that HFET and BAVET should be similarly impacted in V_{TH} for a given change of InAlAs doping. However, the results show a contrary trend. L_{GA_MAX} i- and p-BAVETs differ in V_{TH} by 0.8 V (see Fig. 6.6(b) and 6.7(b)). In HFETs, on the other hand, the gap in V_{TH} increases to as much as 9 V between i- and p-type. The following section posits explanations on this behavior.

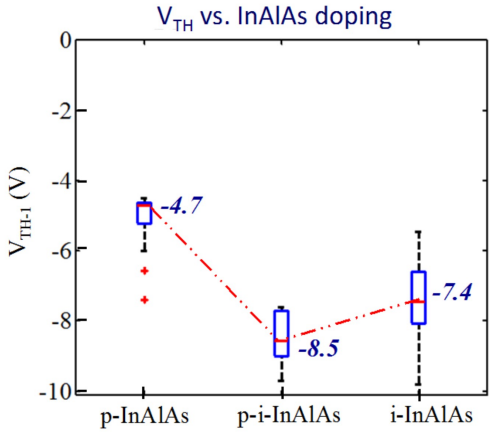


Figure 6.8: Box V_{TH} vs. doping in InAlAs. 13 devices of p, p-i and i-BAVETs are used for each box plot. Each type of BAVET comprises $L_{\mathrm{GA=0}}$. With low standard deviation, V_{TH} can be approximated by median values. V_{TH} changes with InAlAs doping in a manner that is greater than what is expected from a difference in built-in voltage. Additionally, an inverted bell shaped trend implies that pinch-off is a strong function of InAlAs doping.

6.5.1 Factors contributing to V_{TH}

It is possible that the changes in V_{TH} of i-, p-i- and p-BAVETs may not merely reflect the difference in their V_{BI}. But a second factor might contribute to V_{TH} and anomalously change with doping.

Let us first measure the V_{BI} of InAlAs-InGaAs junction as a function of InAlAs doping. It is extracted from capacitance-voltage (C-V) measurements (see Fig. 6.9) [7].

V_{BI} is insignificantly changed between the devices in comparison to V_{TH} vs. InAlAs doping (see Fig. 6.9 and 6.8). For instance, an almost 1 V difference in the V_{BI} of i- and p-diodes is much less than the observed difference of 2.7 V in V_{TH} of $L_{\mathrm{GA=0}}$ i- and p-BAVETs. It is confirmed that V_{TH} is scarcely impacted by V_{BI} but mainly by the pinch-off behavior. Furthermore, the difference in (a) ξ_{CBL} and field-plate effect or (b) impact-ionization and $\xi_{\mathrm{CRIT\_IMPCT}}$, or both is what makes i- and p-BAVETs different in their pinch-off.

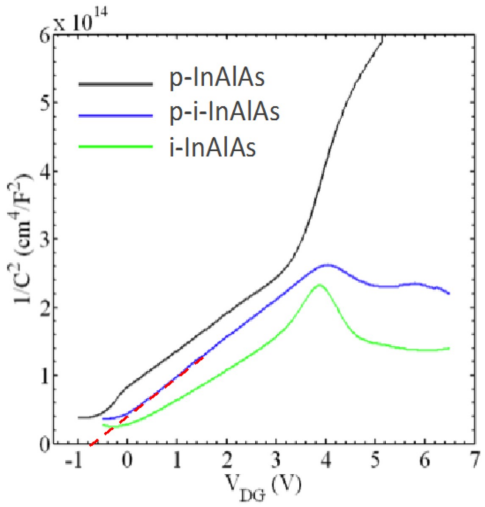


Figure 6.9: $1/C^2$ vs. V measurements is shown for three types of InAlAs-InGaAs diodes. Three diode structures are similar in n-doping of InGaAs but comprise p-, p-i- or i-InAlAs. V_{BI} is the x-intercept of a line fitted to $1/C^2$ in voltage range of constant constant doping. A dashed line fitted to the trace of p-i-diode is shown as an example. The measurements are performed at 1 MHz. V_{BI} for p-, p-i-, and i-diodes is 1.47, 0.7, 0.53 V, respectively.

6.5.2 ξ_{CBL} and ξ_{CRIT_IMPCT}

The results on V_{TH} vs. L_{GA}, L_{AP} and InAlAs doping provide hints with regards to the nature of ξ_{CBL} and ξ_{CRIT_IMPCT} for different types of BAVETs.

With V_{TH} unaffected towards changes L_{GA} and L_{AP} in Fig. 6.6(b) identifies the fact that ξ_{CBL} is independent to any efforts of field plating the p-BAVETs, which is contrary to what is observed for i-BAVETs in Fig. 6.7(b).

Changing doping in InAlAs changes V_{TH} in BAVETs with a given L_{GA} (see Fig. 6.8). It effectively represents that InAlAs doping plays a role in modifying ξ_{CRIT_IMPCT} for a given ξ_{CBL}. A detailed discussion on field plate effect in i-BAVETs can be found in ref. [1]. The following section reports on ξ_{CBL} and ξ_{CRIT_IMPCT} of p-BAVETs.

6.5.3 Phenomena behind pinch-off and V_{TH} in p-BAVETs

V_{TH} of -4.1 V is measured in a p-HFET, a device without an aperture. It is similar to that of a vertical device or BAVET, wherein V_{TH} equals -4.7 V. This leads us to deduce the following three features for p-devices. (i) Neither p-BAVET nor p-HFET impact ionizes at its CBL or drain edge, a generally observed property in p-devices (see Fig. 6.10(a)). (ii) Pinch-off is obtained and it is so without a field-plate effect. $L_{\mathrm{GA\_MAX}}$, $L_{\mathrm{AP>0}}$ or a p-InAlAs disposed over aperture region of channel are ineffective to redistributing field at the drain edge devices (see Fig. 6.10(b)). (iii) A high ξ_{CBL} is, therefore, sustained at drain edge under the pinch-off condition for both p-BAVET and p-HFET.

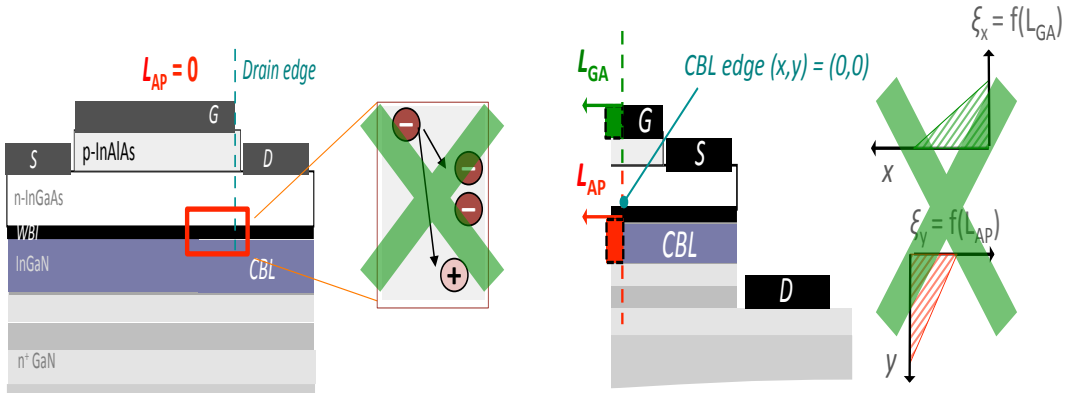
With regards to i-devices and also presented in ref. [1], their behavior is in contrast to p-devices. A generally present weak pinch-off implies that i-devices impact-ionize (see Fig. 6.7). A less negative V_{TH} or strong pinch-off or mitigation of impact ionization is obtainable in one specific case of L_{GA}. i-devices require $L_{\mathrm{GA\_MAX}}$ for field plating and reducing ξ_{CBL}.

In other words, i-device and p-device can both sustain high ξ_{CBL} but one impact-ionizes while the other does not. Such difference can be caused by a change of $\xi_{\mathrm{CRIT\_IMPCT}}$.

6.5.4 $\xi_{\mathrm{CRIT\_IMPCT}}$ in p- vs. i-BAVETs

It was proposed in ref. [1] that i-BAVETs impact-ionize on account of high ξ_{CBL} in a region of low $\xi_{\mathrm{CRIT\_IMPCT}}$. Whereas this work finds that a different type of BAVETs, namely p-BAVETs, do not impact-ionize for high ξ_{CBL}. It is then argued that CBL edge of p-BAVETs must exhibit a high $\xi_{\mathrm{CRIT\_IMPCT}}$. A phenomenon is thus arrived at, wherein a change of $\xi_{\mathrm{CRIT\_IMPCT}}$ is achieved by a change in InAlAs doping, such that $\xi_{\mathrm{CRIT\_IMPCT}}$ increases from an i-BAVET to p-BAVET.

The condition (6.1) between the two BAVETs is formulated for two types of BAVETs.



(a) (b)

Figure 6.10: (a) A cross sectional schematic of a p-HFET. A box in a region comprising drain edge of channel-WBI-CBL is highlighted and a cross mark is used to denote the absence of impact-ionization in the boxed region. (b) Impact of increasing L_{GA} and L_{AP} on the lateral and vertical field distribution at CBL edge of a p-device is shown. A cross mark signifies that LGA and LAP are ineffective to inducing a field-plate effect in p-devices.

The behavior of i-BAVETs is described by:

$$\xi_{CBL} \gg \xi_{CRIT\_IMPCT} \tag{6.2}$$

whereas the equation that represents p-BAVETs is:

$$\xi_{CBL} \gg \xi_{CRIT\_IMPCT} \tag{6.3}$$

Lowering impact ionization of channel-WBI-CBL region by enhancing the region's ξ_{CRIT_IMPCT} is a property that is gained in a p-BAVET.

6.5.5 Critical field of Channel or WBI

As ξ_{CRIT_IMPCT} is a material property of the CBL region comprising channel-WBI, it is likely that either channel or WBI are changed in ξ_{CRIT_IMPCT} by a change of gate-

barrier doping. Irrespective of which one of the two is the limiting feature, it is true that the feature's $\xi_{\text{CRIT\_IMPCT}}$ is raised in a method of p-doping InAlAs. A layer that is placed next to the channel and remotely located with respect to WBI.

The two types of BAVETs shown in Fig. 6.5 are not changed in channel but only in the InAlAs layer. Neither does the doping in InAlAs impacts the channel in its bandgap or $\xi_{\text{CRIT\_IMPCT}}$. It is argued that WBI and its $\xi_{\text{CRIT\_IMPCT}}$, by a remote mechanism, maybe influenced by what doping is used for InAlAs.

The remote mechanism is passivation of traps at WBI. In another study that will be published elsewhere, it is found that p-doping InAlAs is strongly effective in reducing trap activity at the WBI. While traps remain active and unpassivated, if InAlAs is doped unintentionally. We propose that the nature of trap passivation plays a role in determining trap ionization of WBI such that impact ionization of WBI is prevented if its traps are passivated. It is this improved behavior WBI in p-BAVETs that realizes a higher $\xi_{\text{CRIT\_IMPCT}}$.

6.6 Conclusion

The study formulated conditions pertaining two different cases of impact-ionization in a BAVET. In one, impact-ionization was present due to a high ξ_{CBL} in a region of low $\xi_{\text{CRIT\_IMPCT}}$, whereas in the other, gaining a high $\xi_{\text{CRIT\_IMPCT}}$ served to eliminate impact ionization. The work focused on the latter, and found a method to enhance and isolate the region limiting $\xi_{\text{CRIT\_IMPCT}}$.

BAVETs with p-doped InAlAs were compared against those wherein it was unintentionally doped. Devices referred to as p-BAVETs and i-BAVETs, respectively, were fabricated. Tests were also performed to identify field plate effect from L_{GA}, L_{AP} and aperture-extension of p-InAlAs.

It was evident that in the case of p-BAVETs, V_{TH} is neither a function of L_{AP} nor L_{GA}. In other words, field plate effect was either absent or if present had no impact on V_{TH} of p-BAVETs. A property in contrast to that observed for i-BAVETs. A comparison of pinch-off in a p-and i-devices with $L_{\mathrm{AP}=0}$ pointed out another information that impact-ionization was generally absent for p-devices but generally present for i-devices.

Presence of field-plate effect and onset of impact-ionization depended on the choice of doping in InAlAs. In the progress of this work it became clear that impact ionization did not arise due to channel's material property like bandgap. Supported by this and the fact that the electrical activity of traps at WBI was a function of doping in InAlAs, the study proposed the following important property of BAVETs. Pinch-off and impact ionization in a BAVET is determined by $\xi_{\mathrm{CRIT\_IMPCT}}$ of WBI. And in passivating traps, one reduces trap ionization at WBI and raises $\xi_{\mathrm{CRIT\_IMPCT}}$. Using p-doping for the gate-barrier achieves this favorable nature of WBI and so enhances off-state breakdown and pinch-off in a BAVET.

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Chapter 7

Passivation of Traps at a Wafer-Bonded Interface

7.1 Introduction

Junctions by wafer-bonding and their devices can be an alternative to gain performance that is not offered in conventional epitaxy-based junctions and devices.

7.1.1 What is direct wafer bonding?

Direct wafer bonding is a technique by which two or more materials can be stacked together with the formation of a heterointerface called the wafer-bonded interface (WBI). Hereinafter, direct wafer bonding is referred to as wafer bonding. The technique involves taking two semiconductor structures and pressing them against each other at a high temperature (see Fig. 7.1(a), (b) and (c)). The result is a wafer-bonded structure comprising two semiconductor layer structures joined through a WBI (see Fig. 7.1(d)).

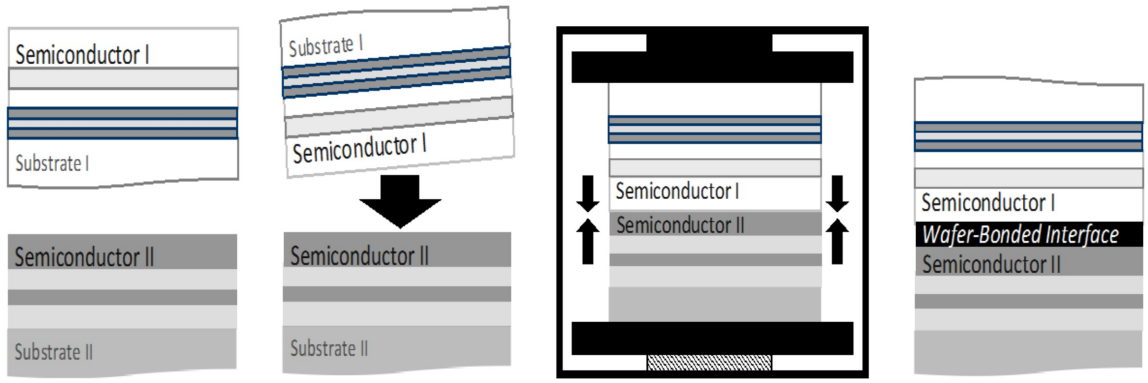


Figure 7.1: (a) A cross section of two semiconductor structures on substrate I and II comprising surface layer semiconductor I and II, respectively. (b) A top-down view illustrating the process of placing inverted semiconductor I structure on top of that of semiconductor II. (c) The stack of two structures is placed between two tool plates (denoted by shaded regions disposed on top and bottom of the semiconductor stack) of a wafer bonding system. Pressure is applied to the tool plates (denoted by shaded arrows) such that the two structures are pressed aginst each other. (c) Cross section schematic of a wafer-bonded structure is shown which comprises a wafer-bonded interface (WBI).

7.1.2 Need for wafer bonding

Every material system is unique in its physical properties like mobility, bandgap, polarization etc. And these properties can have trade-offs. For instance a material with high mobility can lack in bandgap. III-As provides the former while III-N fulfills the role of a wide bandgap material. A structure comprising both III-As and III-N materials is therefore well suited to make a THz transistor have a large breakdown.

Integrating lattice mismatched material systems by hetero-epitaxy is difficult but if done it leads to the undesirable presence of crystal defects throughout the layer structure [1]. Wafer bonding, on the other hand, opens a space of possibilities in what material structures can be stacked together. It firstly comes without restrictions in lattice constant or crystal nature, and so allows a wider range of material systems to be combined. For instance, integration of $In_{0.47}Ga_{0.53}As$ (InGaAs) and Ga(In)N with a lattice constant

mismatch of 46% is made possible by wafer bonding [2], [3]. The extent of defect-rich region may well be limited to a few monolayers of WBI in a wafer-bonded structure, a second advantage in wafer-bonded junctions over heteroepitaxial junctions [4].

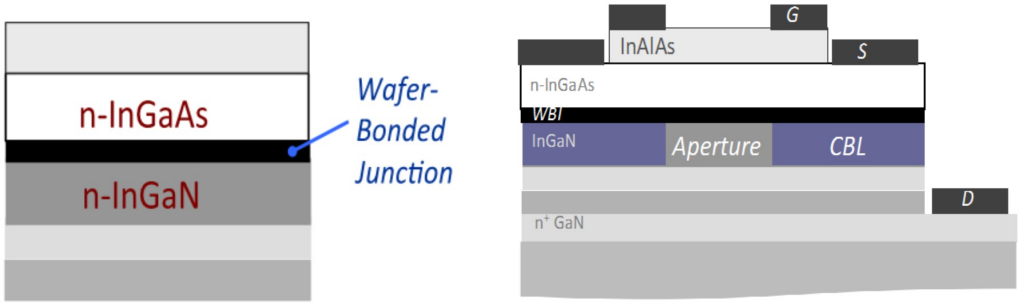
Wafer bonding is widely applied to the device designs of multijunction solar cells, lasers, light emitting diodes (LEDs) and transistors. The operation of these devices requires the WBI to actively participate in current-conduction [5], [6], [7], [8], [9]. The electronic behavior of WBI, thus, plays a fundamental role in achieving the desired operation and performance metrics in the wafer-bonded device.

7.1.3 An ideal WBI behavior in electronic device

The resultant integration of semiconductors by wafer bonding is prone to defect-formation at the WBI. The impact these defects have on the electronic behavior of the WBI can counteract the desired performance benefits of a wafer-bonded device. Eliminating the undesired trap response has been a challenge for wafer-bonded junctions and has been the main cause of non-ohmic behavior in tunnel-junctions, and limiting the forward-bias currents and impacting the turn-on voltages in p-n junctions. Such deviations from the expected response is attributed to trap-induced Fermi-level pinning or/and trap-assisted tunneling recombination phenomena at the WBI [5], [6], [9], [10], [11], [12]. There is however a lack of information on methods which remedy trap response in wafer-bonded junctions.

Understanding the trap activity of an InGaAs-$In_{0.1}Ga_{0.9}N$ (InGaN) WBI is the subject of this study (see Fig. 7.2(a)). It attempts to reduce trap activity, in other words passivate traps, of a WBI. A method to do so is proposed and its applicability in diodes and transistors is reported. Impact of traps is herein studied to rid anomalous behavior in a wafer-bonded current aperture vertical electron transistor, BAVET (see Fig. 7.2(b)). It

is found that the performance of the devices improve dramatically if their WBI is trap passivated.



(a) (b)

Figure 7.2: (a) A cross section of a III-As/III-N wafer-bonded structure showing a WBI between InGaAs and InGaN layers. (b) A cross sectional schematic of a BAVET is shown, wherein InAlAs, InGaAs, III-N region are the gate barrier, channel, and drift regions respectively. Aperture conducts the current vertically while CBL functions as the back-barrier in gate-modulation. WBI interfaces the channel and drift region in aperture and CBL regions. Gate, source and drain electrodes are denoted by G, S, and D, respectively. InAlAs and InGaAs play an additional role in process of passivation of WBI.

7.2 Role of WBI In A BAVET

7.2.1 WBI-related anomalies in a BAVET

A WBI in a BAVET is disposed underneath the channel (see Fig. 7.2(b)). It is an active junction, which interfaces InGaAs to InGaN in aperture and current-blocking layer (CBL) regions. Effects like virtual gate, impact-ionization, drain resistance, have been found to anomalously impact saturation voltage, pinch-off, on-resistance, turn-on voltage, output conductance. It has also been found that majority of these anomalies are local to WBI in either channel-aperture or channel-current-blocking regions of the transistor (see Fig. 7.2(b)).

7.2.2 Traps may cause the anomalies

To identify the property of WBI that regulates a BAVET in most of its device parameters and operation, it is necessary that the trap behavior of WBI be characterized and investigated. If the investigation reveals that a method of trap passivation changes trap activity at WBI as well as eliminates anomalies in a BAVET, then it identifies that it is the traps at WBI that control the device performance. It secondly may furnish a proof of the effectiveness of the method in passivating traps.

The study firstly proposes a method to trap passivation, checks its effectiveness in the case of InGaAs-InGaN WBI. It then investigates if the passivation works to improve BAVETs. A description may too be developed with regards to the design BAVETs while considering the role of WBI traps and passivation.

7.3 A Trap Passivation Method

7.3.1 Principle of a passivation method

Commonly used techniques to reduce the electrical activity of traps in a semiconductor layer structure, are based on the following two requirements: one of them is the presence of a passivation species, and the other is a mechanism to enhance the migration of passivation species from the region of their origin to the region containing traps. These species can interact with the traps and reduce their electrical activity. The phenomenon of reduction in the electrical activity of traps is referred to as passivation of traps and the species performing this passivation of traps are called passivation species.

Hydrogen, deuterium, fluorine, argon, sulfur may be employed as passivation species during growth or fabrication processes. With regards to passivation techniques, they are mainly thermal, chemical, or plasma-based treatments of the semiconductor, which

incorporate the passivation species and assist in the required migration [13], [14]. In another passivation technique, passivation-blocking layers have been added to the structure to preserve the passivation achieved in a prior thermal-treatment [15].

7.3.2 Using hydrogen as the passivation species

Growth and fabrication processes can incorporate significant quantities of hydrogen in a semiconductor, and thus the semiconductor can act as a source of hydrogen [16], [17]. Hydrogen can be present in different forms in the semiconductor like isolated hydrogen, a hydrogen molecule and a hydrogen-based complex. Among these forms of hydrogen, isolated hydrogen – hydrogen not bound to any other species, is the most mobile.

In the majority of semiconductors, isolated hydrogen is known to be amphoteric – it can exist either as H^+ or H^- in most semiconductors. H^+ is present when the Fermi level is close to the valence band (or in a p-doped semiconductor) while H^- is stable when the Fermi level is in the upper part of the band gap (or when the semiconductor is doped n-type) [18], [19]. The mobile nature coupled with the charge-switching capability of isolated hydrogen can be used to advantage in trap passivation. Isolated hydrogen can act as the passivation species, which interacts with the trap, consequently results in trap passivation by forming an electrically inactive and stable complex.

7.3.3 Blocking hydrogen by junction electrostatics

A layer structure may comprise a set of semiconductor-layers, and a trap-containing interface (see Fig. 7.3(a)). The latter is named so for its electrically active traps. Passivation species like hydrogen may be incorporated in the layer structure during growth or fabrication processes. The layer containing passivation species is referred to as the releasing layer (see Fig. 7.3(a)).

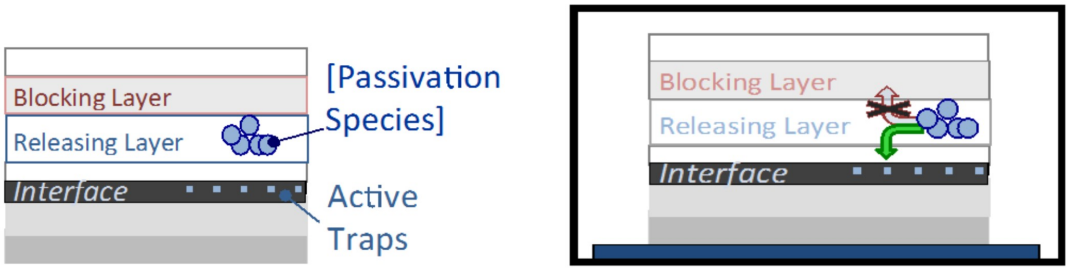
The layer structure comprises of another layer, referred to as blocking layer, which, when disposed in the vicinity of the releasing layer, can provide energy barriers to inhibit migration of passivation species away from the trap-containing region (see Fig. 7.3(a)). In other words, increasing the barrier to hydrogen in one direction causes it to move in the opposing direction.

Energy barrier is herein realized in the build-in voltage or junction electrostatics of releasing and blocking layers. Barrier can be adjusted by changing type of dopants and concentration of either layer.

7.3.4 Thermal process for migrating hydrogen to trap-containing interface

Subjecting the layer structure, which contains the releasing and blocking layers, to thermal processes, can work to enhance the migration of hydrogen (see Fig. 7.3(b)). The two layers are disposed in the layer structure such that the migration through the layer structure is enhanced in a direction towards the trap-containing interface (see Fig. 7.3). Once hydrogen encounters the trap-containing interface, they interact with the traps and results in passivation.

The layer structure and fabrication can thus be designed with following considerations. (a) Add a releasing layer that is likely to be rich in hydrogen. (b) Sandwich the releasing layer between the blocking layer and trap-containing interface. (c) Choose a doping condition such that the blocking layer provides a higher energy barrier. (d) Lastly, the layer structure may be annealed to aid the migration of hydrogen. The present work develops steps (a)-(d) for an InGaAs-InGaN WBI's trap passivation.



(a) (b)

Figure 7.3: (a) A schematic illustration of a semiconductor structure comprising an interface with electrically active traps, a releasing layer containing passivation species and blocking layer. (b) The process of passivation during an anneal is depicted. Upward-directed block arrow denotes the blocking of migrating passivation species in the direction towards blocking layer. The downward-directed block arrow denotes the enhanced migration in a direction towards the trap-containing interface.

7.4 Passivate InGaAs-InGaN Wbi

7.4.1 InGaAs as the releasing layer for H^-

A wafer-bonded structure comprising III-As and III-N layer structures is studied. An n-doped InGaAs layer, which is part of a III-As structure, forms a WBI with an InGaN layer of a III-N layer structure. Both III-As and III-N layer structures are grown by epitaxial techniques (see Fig. 7.4(a)) [20]. Hydrogen is unintentionally incorporated during the growth of InGaAs layer, and exists as H^- in the n-doped layer [19]. H^- plays the role of passivation species, and its source InGaAs acts as the releasing layer (see Fig. 7.4(a)).

7.4.2 Doped InAlAs as a barrier layer

Barrier to H^- is too designed in the III-As structure and disposed next to the n-doped InGaAs. A wider bandgap material like $In_{0.48}Al_{0.52}As$ (InAlAs) comprises blocking layer. It's doping and that of InGaAs together determine the electrostatic barrier for H^-. The

study seeks the doping in InAlAs that obtains a barrier effective to passivation.

7.4.3 Thermal process of wafer bonding

The migration process of H^- is thermally activated during the process of wafer bonding (see Fig. 7.4(b)). It is performed under vacuum conditions at a temperature of ~ 400°C. A pressure of 5 MPa is applied pressing the InGaAs layer of the III-As against the InGaN layer of the III-N for a period of four hours. The InAlAs-InGaAs barrier provides for an electrostatically driven migration of H^- towards the traps at InGaAs-InGaN WBI and so changes its trap activity (see Fig. 7.4(b)).

For a given n-doped InGaAs layer, trap passivation is likely to be enhanced by p-doped InAlAs than that which is unintentionally doped. An experiment is shown herein in which a change of InAlAs doping is performed with the aim of changing or regulating trap activity.

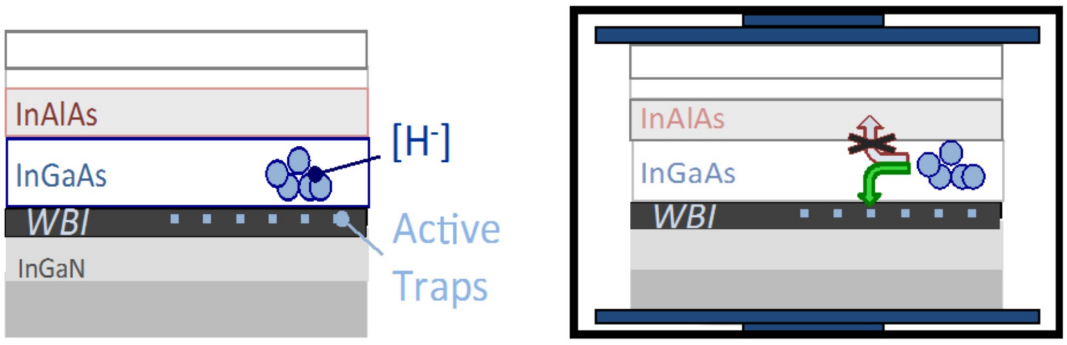
7.5 Experiment

7.5.1 Design three types of barrier layers

Three variations of barrier are studied. Two of which employ p- and unintentional-type doping in InAlAs and are referred to as p- and i-InAlAs, respectively (see Fig. 7.5(a) and (b)). For the third variation, which is called p-i-InAlAs, an interlayer of i-InAlAs is disposed between p-InAlAs and n-InGaAs layers (see Fig. 7.5(c)). The effective barrier to H- at InAlAs-InGaAs junction decreases in the order of p-, p-i, and i-InAlAs.

The three types of III-As structures are wafer-bonded to similar III-N structures. A process, which not only creates a WBI but also, enables trap-passivation.

The III-As substrate in each wafer-bonded structure is removed by wet etch to result in



(a) (b)

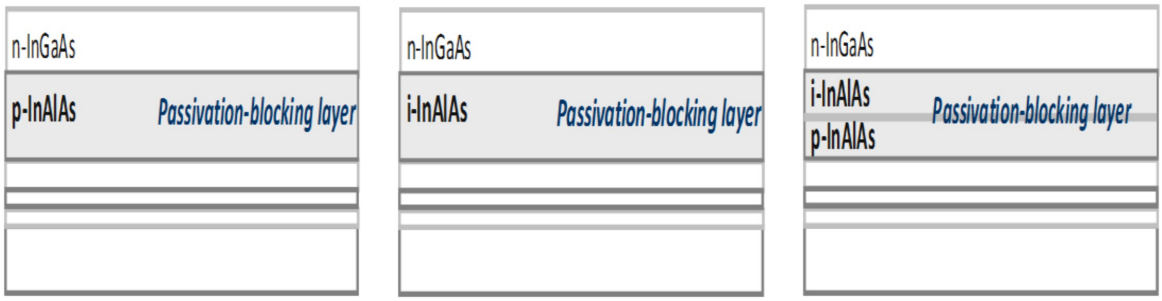
Figure 7.4: (a) A cross section of III-As/III-N structure with InGaAs acting as a releasing and InAlAs as a blocking layer. InGaAs comprises of H^-.Active trap region is confined to WBI. (b) An illustration is shown of the passivation process during wafer bonding anneal. The process is illustrated using block arrows marked in the semiconductor structure, wherein one is directed towards the WBI and the other towards the blocking layer (referred to as downward-directed and upward-directed arrows, respectively). Releasing layer of InGaAs releases H-. The downward-directed block arrow denotes the migration of H- in the direction towards InGaAs-InGaN WBI due to barrier from the blocking layer of InAlAs in the direction denoted by upward-directed block arrow.

a device structure comprising InAlAs, InGaAs and the III-N layers (see Fig. 7.6). InAlAs and InGaAs, the blocking and releasing layers play additional roles of gate-barrier and channel in a BAVET. While its drift region is comprised in III-N layers (see Fig. 7.2(b)). These layers are essential to a device like BAVET [20].

7.5.2 Wafer-bonded diodes and BAVETs to measure a WBI's Trap behavior

Trap-behavior of a WBI can be studied by its electronic-response. For this purpose devices like diodes and transistors are fabricated. The trap-activity of a WBI is deduced from capacitance-voltage (C-V) or current-voltage (I-V) characteristics of diodes and BAVETs.

In order to study trap passivation as a function of InAlAs doping, diodes and BAVETs



(a) (b) (c)

Figure 7.5: Cross section of III-As structures comprising of n-doped InGaAs and three different blocking layer designs: two of the them are designed by doping the InAlAs (a) p-type (denoted by p-InAlAs), and (b) unintentionally (denoted by i-InAlAs). (c) The third design, referred to as p-i-InAlAs, is shown. It comprises an interlayer of unintentionally-doped InAlAs sandwiched between p-InAlAs and n-doped InGaAs. Each structure is inverted and wafer-bonded to III-N structure and tested for differences in WBI trap behavior.

for each type of InAlAs barrier are fabricated and then characterized.

For a given device structure, diodes can be formed that differ in their contact layers. For instance, contacts if formed to the InAlAs and conductive GaN layer yield a diode referred to as gate-drain diode (see Fig. 7.7(a)). A source-drain diode, on the other hand, has its InAlAs layer removed to form one of the contacts to InGaAs layer (see Fig. 7.7(b)). The nomenclature is followed in the manner of their relevance to a BAVET (see Fig. 7.2(b)).

7.5.3 Trap activity on removing blocking layer after wafer-bonding

It was emphasized that a blocking layer is required during wafer bonding to implement the trap passivation method. But whether trap-passivation achieved during bonding is made ineffective on removal of InAlAs after bonding is yet not known. A test of preservation of trap passivation is needed. Secondly, it is also necessary to isolate whether characteristics of diodes represent trap activity at WBI or that of InAlAs-InGaAs interface.

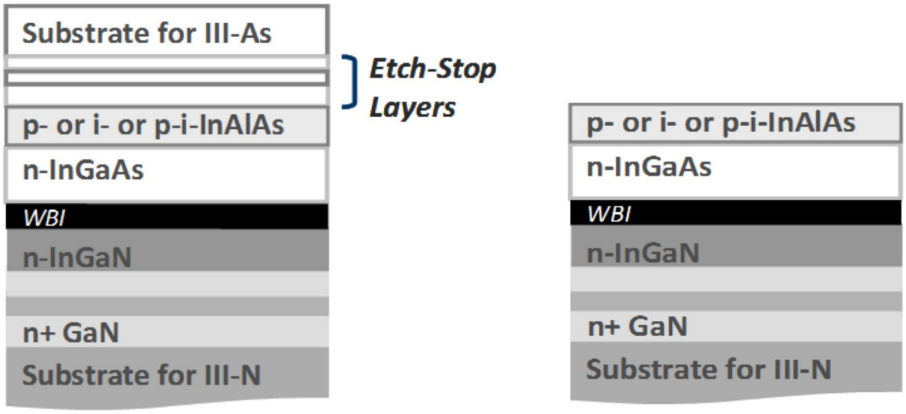


Figure 7.6: Cross sections of III-As/III-N structure: (a) after wafer bonding, and (b) after substrate removal, wherein the III-As substrate and etch-stop layers are removed.

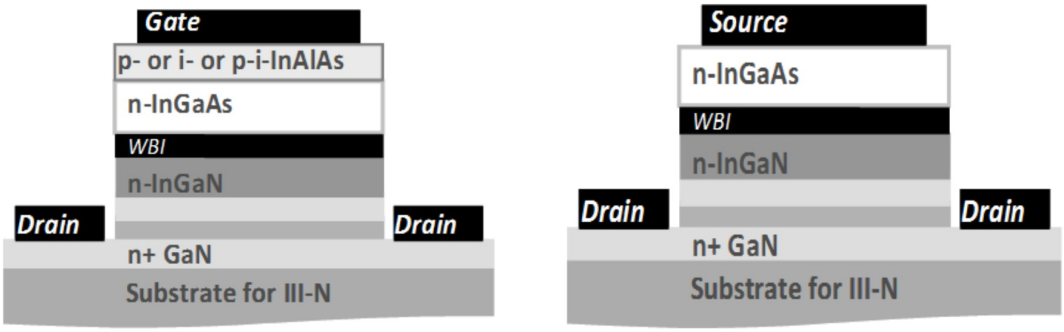
Both these questions are addressed in experiment that compares trap activity of a diode comprising both the interfaces, namely InAlAs-InGaAs and WBI, to that with a diode that contains only WBI. The latter is obtained by removing the InAlAs layer after the step of wafer bonding. This not only removes InAlAs-InGaAs interface but also tests its impact on trap passivation of WBI. The purpose is served in a comparison of gate-drain and source-drain diodes.

7.6 C-V Measurements

Trap activity of WBI is interpreted through C-V and transistor characteristics.

7.6.1 Capacitance-voltage measurements

The quality of the WBI can be evaluated by performing C-V measurement. It is based on the principle that a change in the applied voltage modulates the stored charge in a semiconductor [17], [18]. Applying reverse bias to a junction diode depletes the stored charge, increases the width of the space charge or depletion region, and leads



(a) (b)

Figure 7.7: Schematic illustrations of different types wafer-bonded diodes: (a) Gate-drain diode with gate-contact to the passivation-blocking layer of InAlAs and drain-contact to the III-N layer, (b) The passivation-blocking layer is removed from the device structure in (a) to form the source-drain diode, wherein the source and drain-contacts are formed to the passivation-releasing layer of InGaAs and n+ GaN layer. Both the diodes are structurally also differentiated in their electrodes and InAlAs layer. Additionally, InAlAs is doped p-, or p-i- or i-type for gate- or source-drain diodes. InGaN-GaN junction has been delta n-doped to compensate polarization charges. It can be assumed that diode characteristics mainly probe junction electrostatics of InAlAs-InGaN and WBI than InGaN-GaN.

to a monotonically decreasing capacitance. Increasing depletion width with bias is a consequence of the movement of the Fermi-level across the bandgap with the applied bias. However, C-V trace deviates from the expected behavior when there are trap states in the bandgap as they change their occupancy in response to the sweeping Fermi-level. Additionally, a frequency dependent response in a C-V may arise due to a time constant associated with the traps.

7.7 Results of C-V Measurements

7.7.1 C-V as a function of InAlAs doping

Three source-drain diodes are fabricated on the wafer-bonded structures comprising blocking layers of i-InAlAs, p-i-InAlAs, and p-InAlAs (see Fig. 7.7(b)). Hereinafter, the

three source-drain diodes are referred to as i-, p-i-, and p-source-drain diodes. It should be emphasized that in these source-drain diodes, InAlAs layer is present during the wafer bonding process but is intentionally removed during the fabrication of the diodes. Each of the diode comprises releasing layer, WBI and III-N layers.

With the absence of InAlAs-InGaAs interface, the results of the C-V measurement are expected to be mainly a manifestation of the electrostatics of a WBI. A bias is applied between InGaAs and GaN layers of each of the diode to measure the respective C-V traces. The oscillation signal voltage of 1 MHz is applied.

High-frequency C-V traces of p-, p-i-, and i-source-drain diodes are compared in Fig. 7.8. Capacitance reduces as p-source-drain diode is biased into the depletion regime. However, in contrast, i- and the p-i- source-drain diodes show an anomalous increase in the capacitance, which is most severe in the former.

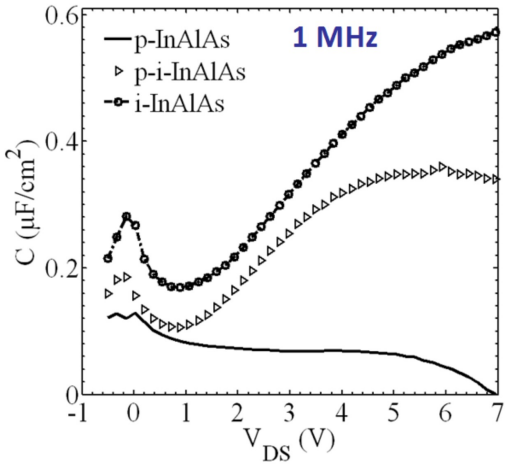


Figure 7.8: p-, p-i- and i-source-drain diodes are characterized. High-frequency (1 MHz) reverse-bias C-V measurements of the WBI for each of the diode show Fermi-level pinning in diodes formed from the structures that contained i-, and p-i-InAlAs. Lowest Fermi-level pinning, and thus lowest electrically active trap density, exists in the diode formed from a structure that comprised of p-InAlAs during wafer bonding.

7.7.2 Frequency-dependence in C-V

A gate-drain diode is characterized for frequency dispersion in a C-V trace. Three types of gate-drain diodes are fabricated from wafer-bonded structures that differ in InAlAs layers. These are referred to as p-, p-i- or i-gate-drain diodes. Unlike the source-drain diodes described earlier, the gate-drain diodes have the blocking layers present in the diode structures (see Fig. 7.6(a) and (b)). A bias is applied between InAlAs and GaN layers of each of the gate-drain diode and C-V traces are measured with frequency as the control-variable. The i-gate-drain diode shows a strongest frequency-dispersion in the depletion-regime of the C-V traces (see Fig. 7.9). It reduces if p-doped InAlAs added like that in a p-i-gate-drain diode. While p-gate-drain diode exhibit the least frequency dependence in C-V.

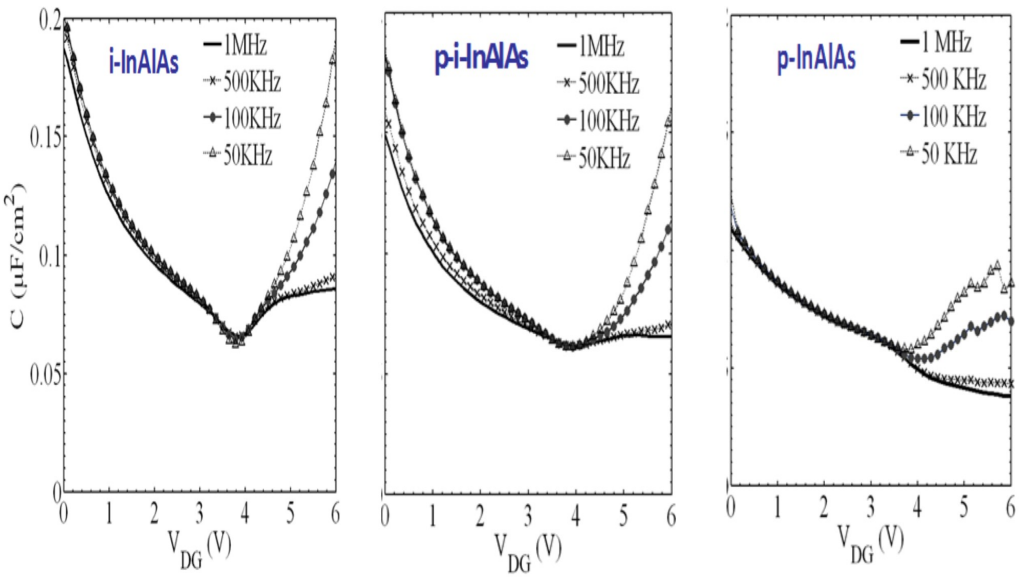


Figure 7.9: (a), (b) and (c) are the reverse-bias C-V responses of i, p-i-, and p–gate-drain diodes, respectively. C-V is measured as a function of frequency. The applied signal-frequency varies as: 50 KHz, 100 KHz, 500 KHz, and 1 MHz. Frequency dispersion in the depletion regime of C-V is highest for the diode that comprised i-InAlAs during wafer bonding. And the dispersion reduces if a p-i-InAlAs or p-InAlAs are used as the passivation-blocking layer during wafer bonding.

7.8 Discussion on C-V Measurements

7.8.1 InAlAs doping influences trap activity of WBI

Incremental trend in the capacitance of i- and p-i-source-drain diodes is observed because the applied voltage is unable to increase the depletion charge but instead charges or discharges the trap states at the WBI. As a result the movement of the Fermi-level is diminished – a phenomenon referred to as Fermi-level pinning. Capacitance increases anomalously as long as the Fermi-level stays pinned. The decreasing trend in the C-V is restored if Fermi-level moves beyond trap states.

The stretch out in C-V behavior becomes higher as well as wider in the order of p-, p-i-, and i-source-drain diodes. Fermi-level pinning is observed to be strongest in i-source-drain diode, which can be attributed to the presence of a larger active trap density at the WBI of i-source-drain diode in comparison to the WBIs in p-i- and p-source-drain diodes.

The WBI of p- source-drain diode which had the highest electrostatic-barrier to H- has, as a result, led to a lowest electrically-active trap density relative to both the p-i and i-source-drain diodes. Additionally, a distinctive trend is observed, wherein a steady reduction in the active trap density at WBI with the increase in InAlAs-InGaAs barrier from i- to p- through p-i-InAlAs. It is proposed that the trap density at the WBI can be passivated by both the approaches, namely: using p-doped InAlAs as well as by the use of an interlayer of i-InAlAs between p-InAlAs and InGaAs layers. The latter is less effective than p-doped blocking layer.

7.8.2 Improved Trap passivation at WBI of p-doped InAlAs

If on lowering the frequency the depletion capacitance is shifted to higher values and the stretch out in the C-V trace is widened, then it is a proof of a trap-induced Fermi-level pinning as the frequency is lowered. It is so observed for i-gate-drain diodes (see Fig. 7.9(a)). The dispersion phenomenon is however mitigated in the C-V of the p-i- and p-gate-drain diodes (see Fig. 7.9(b) and (c)). This is another confirmation of the presence of less electrically active traps at WBI when using p-doping and/or p-i-doped InAlAs-based electrostatics to enhance hydrogen-based passivation.

7.8.3 Trap-passivation unaffected by a post-bonding InAlAs removal

Both p-gate-drain and p-source-drain diodes show reduced trap-induced Fermi-level pinning. Low trap activity is present despite a difference in their layer structure. The passivated nature of the WBI survives the removal of the blocking layer in a fabrication step subsequent to the wafer bonding process. Conversely, it serves the proof that active trap density of an InGaAs-InGaN WBI can be controlled during the thermal process of wafer bonding. Measurement results render the correctness of the argument that hydrogen-based passivation is adjusted by changes to InAlAs blocking barrier and that wafer bonding is the enabling step.

7.9 WBI in A BAVET

7.9.1 Operation of a BAVET & role of WBI traps

In a BAVET's on-state operation electrons transit laterally through InGaAs, which is sandwiched between InAlAs and WBI-CBL. Applying gate voltage changes the channel

conductivity in the WBI-CBL region (denoted by L_{GO} in Fig. 7.10). Once the electrons exit the L_{GO} region, the applied drain voltage pulls them towards the InGaN aperture, through the WBI.

On-state saturation and off-state pinch-off in a BAVET are features that are determined by CBL and aperture regions [9], [20]. With a WBI extending over both CBL and aperture regions, the properties of WBI can additionally influence a BAVET's performance.

In a set of studies, to be published elsewhere, transistor characteristics of BAVETs have shown certain anomalous nature in their performance. Those studies have also isolated WBI to be the cause of such anomalies. It is herein argued that if anomalies in a BAVET are related to WBI's trap-related properties, then in passivating traps one should be able to overcome the limitations in transistor's performance. In the following section, the WBI-passivation method that is developed herein is applied to a BAVET and its results are reported.

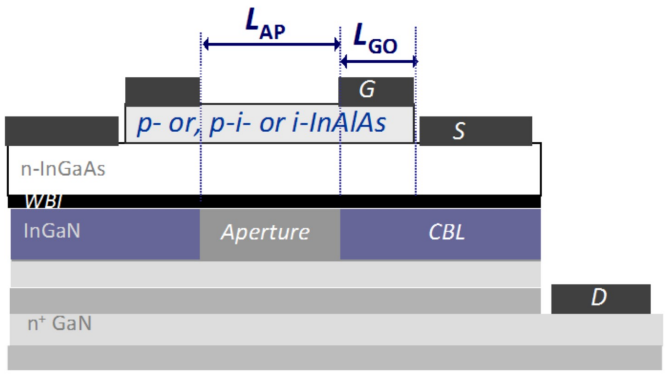


Figure 7.10: Cross section schematic of a BAVET is shown. L_{GO} dimension is used to denote the region of InGaAs channel modulated by the gate. The length of aperture is marked by L_{AP}. WBI interfaces the channel and InGaN in both L_{GO} and L_{AP} regions. For this study three types of BAVETs are fabricated that comprise p-, p-i- or i-InAlAs and are referred to as p-, p-i-, and i-BAVETs, respectively.

7.9.2 Structure of BAVET to study influence of passivation

From the aforementioned discussion on InGaAs-InGaN WBI, it is understood that in the case of a BAVET, the InGaAs channel can be the releasing layer containing hydrogen as the passivation species. InAlAs blocking layer is a gate-barrier. BAVET structure is formed by the wafer-bonding step that also works to passivate WBI.

The experiment of changing InAlAs doping from i- to p-type through p-i-type is also performed for BAVETs. Three types of BAVETs are fabricated, namely, i-, p and p-i-BAVETs (see Fig. 7.10). Each BAVET is characterized for its I-V_{DS} characteristics and compared with the other to identify the change in I-V_{DS} traces due to the change of trap passivation.

7.10 Results of Bavet Performance Vs. InAlAs Doping

7.10.1 Transistor I-V characteristics

A WBI is disposed in the vicinity of source and drain edges of the channel of a BAVET. A trap-affected vs. a trap-passivated WBI must yield differences in characteristics of corresponding BAVETs. The results of i, p-i and p-BAVETs are shown herein for the purpose of identifying and understanding their differences.

Fig. 7.11 shows the source-current (I_{S}) vs. drain-voltage (V_{DS}) characteristics of three types of BAVETs. Applying p-doped InAlAs improves I_{S}-V_{DS} characteristics, especially in its current saturation and pinch-off behavior.

7.10.2 On and off-state performance vs. InAlAs doping

The multiplicity and magnitude of performance changes is classified into device parameters shown in Fig. 7.11, wherein each parameter is extracted from I-V measurements and plotted against InAlAs doping. Method of extraction is detailed in ref. [21]. A strong dependence of each parameter on the latter is shown. The dependence that may shed light on what causes I-V characteristics to improve in p-BAVETs.

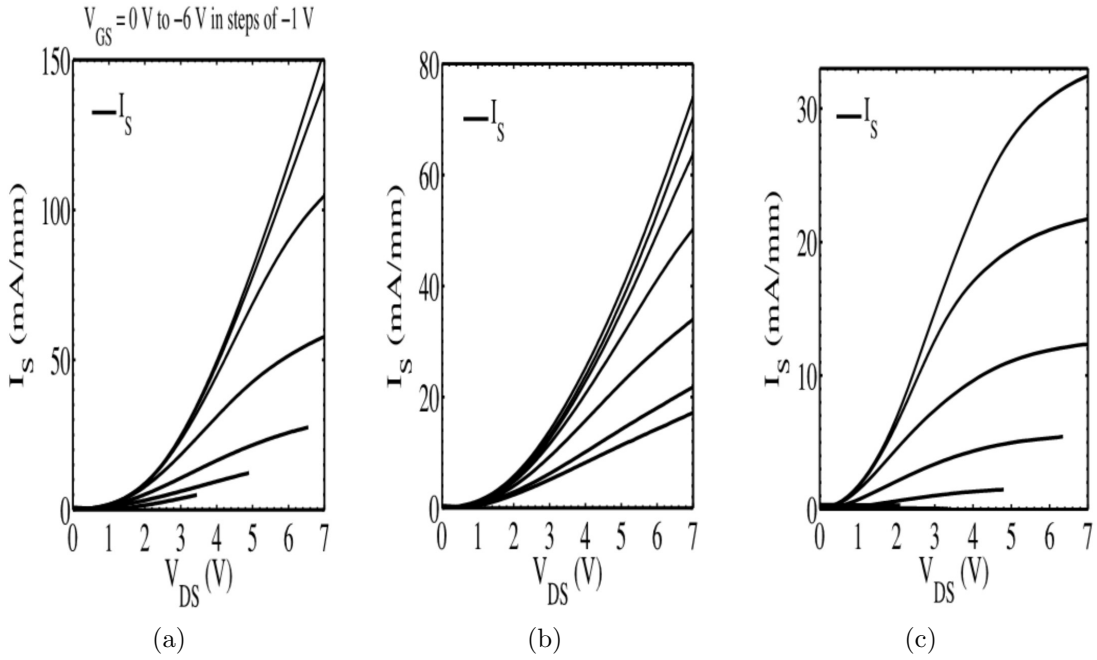


Figure 7.11: I_S-V_{DS} traces are shown for (a) i-, (b) p-i-, and (c) p-BAVETs. These are measured as a function of gate-voltage (V_{GS}) varying between 0 V to -6 V, in steps of -1 V. Performance in both on-state saturation and off-state pinch-off is a strong function of InAlAs doping.

Between i- and p-BAVETs, on-state saturation in the former on one hand requires higher V_{DS} (referred by saturation voltage - V_{DS_SAT}) and on the other it is made weak by higher output conductance (G_{OUT}) (see Fig. 7.12(a) and (b)). Turn-on voltage (V_{DS_ON}) and drain resistance (R_X) are the other two factors influencing on-state performance. Lower V_{DS_ON} and R_X make a well-behaved I-V trace in a transistor, a feature available

for p-BAVETs but weakly present in p-i and i-BAVETs (see Fig. 7.12(c) and (d)).

Obtaining off-state pinch-off is a necessary condition in a transistor's operation and also complements its breakdown characteristics. Threshold voltage (V_{TH}) monitors pinch-off such that if V_{TH} is highly negative then it is likely due to a weak pinch-off. V_{TH} is most negative for p-i-BAVETs and least for p-BAVETs.

It is stated that in i- and p-i BAVETs, the anomalous nature of their I_S-V_D traces arises due to a large set of device parameters being anomalous. In contrast, p-BAVETs respond with a well-behaved transistor I_S-V_D trace mainly because of the absence of anomalies in all of the above mentioned parameters.

InAlAs doping changes the built-in voltage (V_{BI}) of the InAlAs-InGaAs junction is changed. V_{BI} decreases from 1.47 V in p-BAVETs to 0.7 and 0.53 V in p-i-, and i-BAVETs, respectively. In addition to changing V_{BI}, the doping of InAlAs has been found in this work to also effect trap behavior of InGaAs-InGaN WBI. The question then arises whether it is the InAlAs-InGaAs junction and its V_{BI} or InGaAs-InGaN WBI's trap behavior that changes the nature of anomalies in characteristics of a BAVET.

7.11 Discussion On Wbi Passivation In BAVETs

7.11.1 Anomalies represent anomalous behavior of WBI

A detailed analysis on V_{DS_SAT}, R_X, V_{TH} vs. InAlAs doping has been presented in ref. [21], [22], and [23], respectively. From the large inequality between how each parameter changes with respect to that expected by the change of V_{BI}, it was hinted that WBI might be the primary factor regulating V_{DS_SAT}, R_X and V_{TH}. Additional deductions were made, namely (a) an anomalously high V_{DS_SAT} is a response of a virtual gate buried in WBI region of BAVETs. (b) The behavior of WBI in the aperture region furnishes the drain

resistance of R_X. (c) Critical field of WBI if low can lead to its impact-ionization and so cause large negative values of V_{TH} in a BAVET.

Although the studies arrived at three different phenomena of virtual gate, drain resistance, low critical field, yet it isolated a common feature that the anomalies in device parameters are local to WBI and depend on its properties. What property or properties of WBI regulate the performance of a BAVET are yet not known but reported next.

7.11.2 WBI Trap Passivation determines BAVET performance

In prior works it was also proposed that anomalous phenomena (a), (b) and (c) of virtual gate, drain resistance, and low critical field, respectively are mitigated for p-BAVETs. But these effects are dominantly present in i- and p-i-BAVETs. Any change to WBI behavior changes the performance of a BAVET.

A high trap activity at WBI of i- and p-i-diodes is identified in an earlier part of this study on wafer-bonded diodes. An increase in trap passivation or reduction in trap activity is also confirmed for diodes with p-type InAlAs. A reduction of trap activity in WBI of diodes if correlated to the reduction of anomalies in WBI of BAVETs suffices new information. It proves that the performance of a BAVET is tightly related to trap-related properties of WBI. Higher the trap passivation of WBI, better the DC and frequency dispersion characteristics in BAVET and diodes.

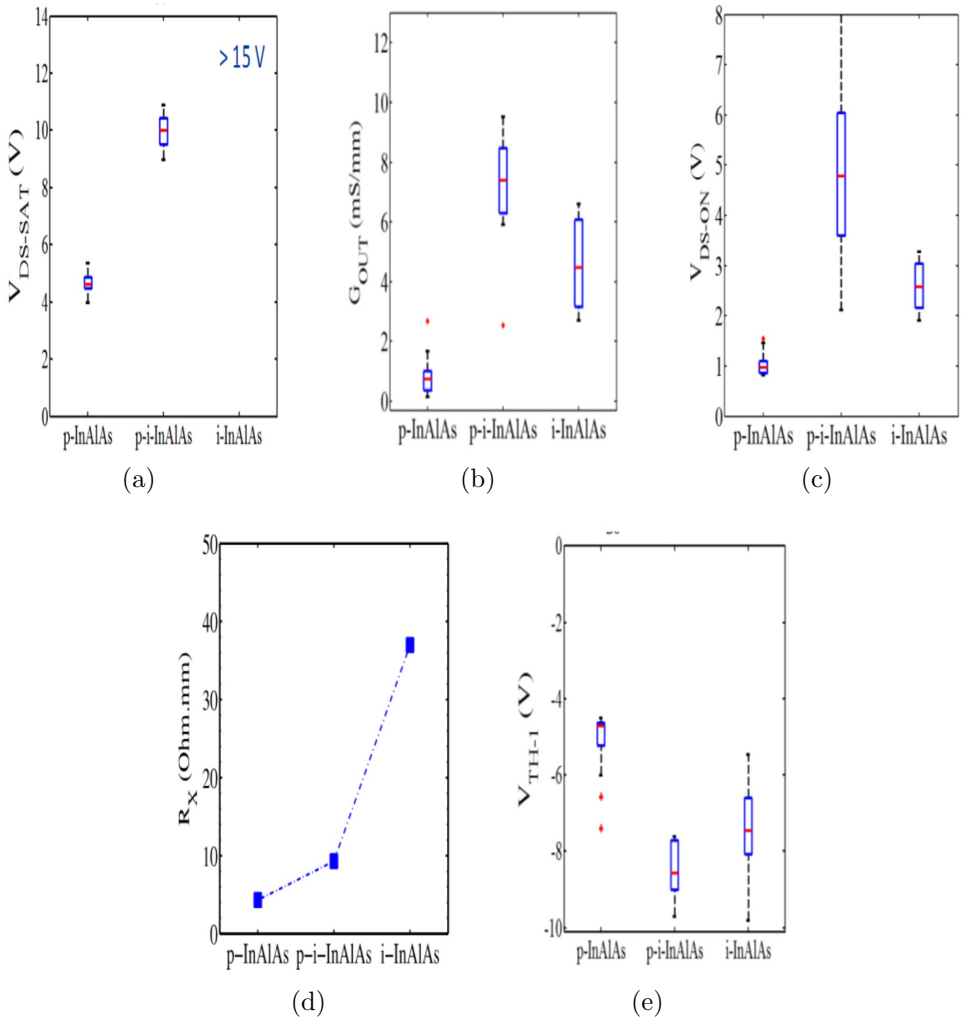


Figure 7.12: (a) $V_{\mathrm{DS\_SAT}}$, (b) G_{OUT}, (c) $V_{\mathrm{DS\_ON}}$, (d) R_{X}, and (e) V_{TH} are plotted against InAlAs doping. (a)-(c) and (e) are expressed in box-plot forms whereas R_{X} is represented by median value. These are extracted from I_{S}-V_{DS} and I_{S}-V_{GS} traces of p, p-i and i-BAVETs. High anomalous values of these parameters are obtained in i- or p-i-BAVETs. On the contrary, minima of $V_{\mathrm{DS\_SAT}}$, G_{OUT}, $V_{\mathrm{DS\_ON}}$, R_{X}, and magnitude of V_{TH} vs. InAlAs doping are obtained for a p-BAVET. The difference in each parameter is not equivalent to changes expected by change of built-in voltage by InAlAs doping.

7.12 Conclusion

WBI, a junction formed by wafer bonding between two similar or dissimilar materials, can be prone to the presence of large electrically active trap density. Such trap behavior was shown to result in poor performance in wafer-bonded diodes and BAVETs. For instance, a high trap activity led to Fermi-level pinning causing high frequency dispersion in diodes. With regards to BAVETs, anomalies in its device characteristics were, too, correlated to trap-related effects of a strong virtual gate, high drain resistance and low critical fields. The study attempted to realize well-behaved diode and transistor characteristics by addressing the trap-related issues of WBI.

For the purpose, a method was presented to reduce electrical activity of traps or enhance their passivation at WBI. It used H^- species of an InGaAs layer for interacting and passivating traps during the process of wafer bonding. Increasing hydrogen-blocking barrier in InAlAs was suggested as the means to enhance the migration of H^- in the direction of WBI. The argument of higher barrier to higher passivation was then tested in an experiment that fabricated wafer-bonded structures differing in InAlAs doping. InAlAs if p-doped posed as a high barrier layer while the barrier strength decreased if structures comprised either p-i- or i-InAlAs layers. In each of three structures, trap behavior was derived from measurements on diodes and BAVETs.

C-V measurements found that Fermi-level pinning and frequency dispersion are nearly absent for diodes with p-doped InAlAs while being dominant for p-i- and i-diodes. Using p-doped InAlAs proved to be extremely beneficial in reducing trap behavior at the InGaAs/InGaN WBI. The method of passivation proved effective for a specific doping design.

Trap passivation remained unaltered on removal of InAlAs if followed by wafer bonding. This experiment isolated the fact that trap passivation requires wafer bonding to

be performed in the presence of a p-InAlAs layer. It being rendered insignificant in post-bonding fabrication steps allows the flexibility of fabricating devices that are with or without InAlAs.

The work also comprised a study that correlates anomalies in BAVETs to WBI's trap behavior. Anomalies impacting on-state and off-state performance of BAVETs were eliminated if the gate-barrier of InAlAs is doped p-type. This result and that of diodes confirmed that traps of WBI must be passivated to improving electronic response, both DC and frequency-response, of a WBI-based device.

The study on InGaAs-InGaN WBIs has recently been extended to other junctions like InGaAs-GaN, N-polar InGaAs-InGaN, and with other variants of p-doped gate barrier like InGaAs [4]. These junctions and devices have shown similar advancements with the use of passivation described herein.

The work made a significant advancement in designing high quality wafer-bonded heterojunctions with applications in solar cells, LEDs, lasers, transistors etc.

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Chapter 8

Conclusions

The dissertation extends to different aspects of wafer-bonded semiconductor devices. It identifies key problems, reports performance enhancements, proposes novel device physics and properties and establishes certain methods of analyzing and resolving the challenges.

8.1 Problem Statements and Experiments

8.1.1 Identifying Design Features

A Wafer-bonded unipolar vertical transistor, herein referred to as a BAVET, functions as a transistor due to certain features. The study focuses on finding these features, and their design for a BAVET. Three experiments are conducted, namely a perture, current-blocking layer (CBL) and wafer-bonded interface (WBI) experiments. Different ways of n-doping the aperture, ion implanting the CBL, and doping the gate-barrier are investigated.

8.1.2 Examining Anomalous Nature of Saturation Voltage

High saturation voltage ($V_{\mathrm{DS\_SAT}}$) has been a limiting feature in BAVETs. We suggest an explanation for this anomalous nature of $V_{\mathrm{DS\_SAT}}$. The study is based on analyzing $V_{\mathrm{DS\_SAT}}$ in three types of BAVETs, which differ in the doping of their gate-barriers.

8.1.3 Investigating weak off-state pinch-off

A study is performed on the pinch-off in wafer-bonded current aperture vertical electron transistors, referred to as BAVETs. Weak pinch-off causes anomalously large negative threshold voltage (V_{TH}) in BAVETs.

Experiments find that pinch-off and V_{TH} represent the behavior of critical field to impact ionization ($\xi_{\mathrm{CRIT\_IMPCT}}$). If it is raised an improvement in pinch-off is also achievable. A condition that is delivered in an experiment of changing the doping of gate barrier.

8.1.4 Localizing the performance limiting feature

The experiments on saturation and threshold voltages lead to the deduction that there is a singular cause of their anomalies. WBI is revealed as a performance-limiting feature in a BAVET.

8.1.5 Improving WBI Behavior to Enhancing BAVET's Performance

Wafer bonding advances semiconductor devices to employing junctions between materials with diverse physical properties. However, little is known on the trap activity of such interfaces and their relationship to the performance of an electronic device.

This work presents some investigations, which have confirmed a key understanding that a wafer-bonded interface (WBI), having electrically active traps, can be dominant source of anomalies in devices.

The deduction is made from capacitance-voltage measurements of WBI-comprising diodes. That this activity of traps can be changed or they can be passivated during wafer bonding is shown in the following way. The structure undergoing wafer bonding is comprised of two doped layers, while one provides hydrogen ions and the other electrostatically aids to enhance interaction between ions and traps.

8.2 Performance Enhancements

8.2.1 DC Transistor Behavior

The aperture experiment yields that δ-n-doping the polar InGaN-GaN interface is ideal for high aperture conductivity. CBL as a current-blocking region is shown to be least leaky if ion-implanted at energies of 53 and 63 KeV. Thirdly, the electronic properties of InGaAs-InGaN WBI are made less anomalous by p-doping of InAlAs. The designs of aperture, CBL and WBI result in a transistor operation realized for the first time in a BAVET.

The device is shown to improve in its overall DC characteristics through improvement in different parameters like maximum on current ($I_{\mathrm{D_MAX}}$), transconductance (g_m), output conductance, saturation and turn-on voltages. The first transistor demonstration in a BAVET is achieved. The work achieves a g_m of 132 mS.mm^{-1}, $I_{\mathrm{D_MAX}} = 600$ mA.mm^{-1}, on resistance of 3 mΩ.cm^2, room temperature channel mobility of 6000 cm^2.V^{-1}.s^{-1} and breakdown voltage between 20-25 V.

8.2.2 On-State Behavior and Saturation Voltage

$V_{\mathrm{DS\_SAT}}$ that determines the onset of on-state saturation regime is made nearly ideal in a BAVET with p-InAlAs. Instead of p-i and i-doping, the use of p-doping in the gate-barrier eliminates an anomalous virtual gate effect in on-state and a corresponding abnormality of high $V_{\mathrm{DS\_SAT}}$.

8.2.3 Off-State Pinch-off and Threshold Voltage

A field-plate effect is revealed from the comparison of V_{TH} in devices differing in their gate-aperture overlap (L_{GA}) and aperture length (L_{AP}).

In reducing peak field or ξ_{CBL}, improvements in pinch-off and threshold voltage are gained. It is firstly able to pinch-off without impact ionizing and without needing a field plate. A change of doping in InAlAs from unintentional to p-doping, on the other hand, reduces impact-ionization or raises $\xi_{\mathrm{CRIT\_IMPCT}}$. A change of both ξ_{CBL} and $\xi_{\mathrm{CRIT\_IMPCT}}$ enhances breakdown, pinch-off and reduces anomalous nature of V_{TH}.

8.2.4 Trap Activity at WBI

Enhanced trap passivation at WBI is achieved for p-type doping in remotely located gate barrier layer. Differences in doping type this layer yields differences in trap activity or passivation. Trap passivation eliminates certain performance anomalies and so improves the DC characteristics of a BAVET.

8.3 Device Physics and Properties

8.3.1 Polarization, Fermi-Level Pinning and Trap Activity

Phenomena related to polarization, ion-implantation-induced and WBI defects are observed.

Turn-on voltage and on resistance depend on WBI trap behavior and aperture conductivity, respectively. The former is reduced by passivation and doping against polarization improves aperture conductivity. Output conductance is found to depend partly on a WBI and partly on the back-barrier of CBL. The concept of Fermi-level pinning is proposed to work in making the CBL barrier effective and so realizing g_m in the transistor.

Aperture doping and CBL ion-implantation energy affected the regions locally. BAVETs, however, responded to change in doping of the gate-barrier in the most unexpected manner. It impacted regions that are not only localized near the gate-barrier but also situated remotely like WBI-aperture, WBI-CBL-aperture edge and WBI-CBL.

The study, thus, (a) confirms the role of aperture, CBL and WBI in operation and performance of a BAVET, (b) relates polarization phenomenon to aperture conductivity, the effect of Fermi-level pinning in CBL to regulate leakage and g_m, and trap activity at WBI to overall behavior of the transistor.

8.3.2 A Virtual Gate Induced by Traps at WBI

The study made progress in understanding on the mechanism controlling $V_{\mathrm{DS\_SAT}}$. It is proposed by comparison of BAVETs differing in InAlAs doping that anomalous nature of $V_{\mathrm{DS\_SAT}}$ is a response of a buried virtual gate. Specifically, traps induce a virtual gate at WBI-CBL-Aperture edge, the electrostatic potential of which influences the V_{TH} at drain edge, or $V_{\mathrm{TH\_DRAIN}}$, of the transistor and so regulate $V_{\mathrm{DS\_SAT}}$. The presence of

virtual gate is a strong function of trap activity at WBI. Lower trap activity eliminates the virtual gate.

The work established that the behavior of WBI determines the relationship between the threshold voltages at source ($V_{\mathrm{TH\_SOURCE}}$) and drain. A trap affected WBI may have a $V_{\mathrm{TH\_DRAIN}}$ that is not equivalent to $V_{\mathrm{TH\_SOURCE}}$ in a long channel device, a fact that deviates from that of a long-channel field-effect transistor.

8.3.3 Critical Field of a BAVET, a function of Trap activity at WBI

The peak and critical electrostatic fields, ξ_{CBL} and $\xi_{\mathrm{CRIT\_IMPCT}}$, respectively of the drain edge, govern impact ionization-related breakdown of a BAVET. Experiments prove that either a high ξ_{CBL} or a low $\xi_{\mathrm{CRIT\_IMPCT}}$ can be the breakdown-limiting condition. ξ_{CBL} depends on the electrostatic field distribution whereas $\xi_{\mathrm{CRIT\_IMPCT}}$ is a characteristic of WBI or channel regions in the vicinity of current-blocking layer and not the aperture region.

A low $\xi_{\mathrm{CRIT\_IMPCT}}$ requires that ξ_{CBL} be made low, too, a condition that is shown to be obtainable in redistribution of fields through L_{GA} and L_{AP}. Increasing the two dimensions realizes an enhanced field-plate effect necessary to maintain off-state pinch-off in the device.

This work furthers answers on how to improve off-state performance in a BAVET. It is deduced that (a) enhancing $\xi_{\mathrm{CRIT\_IMPCT}}$ is necessary than reducing ξ_{CBL} and (b) $\xi_{\mathrm{CRIT\_IMPCT}}$ is a property determined by the ionization behavior of WBI, instead of channel.

A method is then conceived to favorably enhance the material property of $\xi_{\mathrm{CRIT\_IMPCT}}$ of WBI and in this way the study successfully achieves an elimination of off-state impact

ionization in a BAVET. The method works to passivate traps at WBI and inadvertently improves pinch-off in a BAVET. Trap behavior is thus also linked to breakdown of WBI and BAVET.

8.4 Methods

8.4.1 Finding Design Features

The design of aperture and CBL enhanced gate modulation characteristic of the transistor but the two features are found to be insufficient to bringing the transistor characteristics to near ideal behavior. This evidence pointed to the presence of a third unknown feature and so required a method of finding it.

Measurements of a number of device parameters presented anomalies in their characteristics. The method of finding the design feature required individually analyzing each parameter, characterizing it in different sets of device types, layouts and structures, then correlating the measurements, accurately proposing underlying device physics and isolating the region that causes the anomalous behavior. This methodology yielded that all the parameters are impacted in their behavior by the trap properties of WBI, and thus a third design feature in a BAVET is found.

8.4.2 Relating the Presence of Virtual Gate to Anomalous Saturation Voltage

An analysis approach is developed to effectively isolate different factors determining $V_{\mathrm{DS\_SAT}}$. It is statistically extracted from I-V_{DS} traces measured for a set of BAVETs. It is then split into components pertaining to turn-on voltage ($V_{\mathrm{DS\_ON}}$), on-resistance and $I_{\mathrm{D_MAX}}$. A comparison of devices differing in InAlAs doping brings out $I_{\mathrm{D_MAX}}$ as the

primary factor regulating $V_{\mathrm{DS\_SAT}}$. This primary factor is then further broken down into its relationships with $V_{\mathrm{TH\_SOURCE}}$ and $V_{\mathrm{TH\_DRAIN}}$ through C-V and TLM measurements. With $V_{\mathrm{TH\_DRAIN}}$ isolated as the key factor, WBI-CBL-Aperture or drain edge of the device is found to be the region of abnormality. Temperature-based I-V_{DS} measurements are used for the next step to confirm the underlying phenomenon of $V_{\mathrm{TH\_DRAIN}}$'s anomalous nature. This process of elimination tests the cause against either impact-ionization or virtual-gate effect.

8.4.3 Isolating the Role of WBI's Trap Ionization in Critical field of BAVET

The study on anomalous nature of V_{TH} and pinch-off (a) furnishes us a method that isolates the breakdown-limiting feature and (b) develops a description on how to regulate peak field in a BAVET. The method of analysis tests pinch-off, firstly, for its causal phenomena like drain-induced barrier lowering, gate leakage and impact ionization and secondly, for the causal factors of peak and critical electrostatic fields, ξ_{CBL} and $\xi_{\mathrm{CRIT\_IMPCT}}$, respectively.

Impact-ionization in the drain regions of device is proved to be the pinch-off limiting phenomenon. This information is yielded by comparison of drain-current injection method measurements in near pinch-off regime for devices differing in L_{GA}. Statistically derived V_{TH} medians are measured against L_{GA} and L_{AP} as the means of studying pinch-off's dependence on ξ_{CBL}. Varying L_{GA} and L_{AP} introduces a difference in field plate effect and so works to modify ξ_{CBL}. The experiment not only tests ξ_{CBL}, but also hints on its relative magnitude with $\xi_{\mathrm{CRIT\_IMPCT}}$. Devices are in this way tested for different ξ_{CBL} for a given $\xi_{\mathrm{CRIT\_IMPCT}}$. The method acts as the means to modify ξ_{CBL}. Studying pinch-off or V_{TH} in a devices with L_{AP} of either non-zero or zero presents the opportunity

of isolating between aperture and CBL as the region that impact-ionizes.

Testing another set of devices, wherein the InAlAs doping is changed furnishes the method of testing pinch-off for a given ξ_{CBL} but different $\xi_{\mathrm{CRIT\_IMPCT}}$. The study realizes a way to modify or regulate $\xi_{\mathrm{CRIT\_IMPCT}}$. This line of investigation also attempts to eliminate built-in voltage as the factor impacting V_{TH}. And the fact that the experiment that changes $\xi_{\mathrm{CRIT\_IMPCT}}$ does so without a change in channel material confirms that $\xi_{\mathrm{CRIT\_IMPCT}}$ is material property set by trap-ionization of WBI and not the impact ionization of channel.

8.4.4 Linking Trap Behavior of WBI to Performance of BAVET

With WBI being the key design feature and also its trap being the cause of anomalies in device parameters like saturation voltage and pinch-off, it required to be studied whether trap behavior of WBI yields anomaly-free BAVET. The investigation acts as the method to link the electronic behavior of a WBI and a BAVET.

The argument is tested by correlating on- and off-state behavior of a BAVET in WBIs that differ in their trap behavior. Analysis firstly, isolates the effect that a device with high trap activity at WBI also has the most anomalous nature in BAVET characteristics. A BAVET behaves poorly on account of trap activity. It thus establishes the link between trap activity at WBI with anomalies in BAVET's performance.

The process of investigation thus works to confirm the performance-limiting feature in wafer-bonded devices and additionally proposes and demonstrates a passivation method to improve the feature's electronic behavior. In applying the technique of passivation to BAVETs, the work not only proves its effectiveness to reduce trap activity at WBI but also improves the performance in different device parameters of a BAVET. For instance, the methodology eliminates anomalies pertaining to $V_{\mathrm{DS\_SAT}}$, $V_{\mathrm{DS\_ON}}$, RON, output con-

ductance, V_{TH} and enhances the transistor behavior in both on- and off-state.

Chapter 9

Future Work

The dissertation opens up a space of possibilities in three areas of exploration. One of these may focus on advancing InGaAs/III-N BAVET performance to meeting the goal of a THz power transistor. Applying wafer-bonded junctions to other electronic applications may be a second opportunity. A third aspect of investigation can be based on employing other material systems,like oxides and nitrides, to wafer-bonded devices other than transistors like light-emitting diodes, lasers etc.

9.1 Possible Solutions to Performance Enhancements

9.1.1 Increasing Transconductance

Higher transconductance (g_m) in a BAVET is necessary to enhance its potential as a high frequency transistor. It was found that the ion-implant energy of CBL plays a role in determining g_m. An underlying phenomenon is likely the compensation of channel dopants by the implanted ions of CBL. Capacitance-voltage (C-V) characteristics and related charge profile have shown such compensation. Changing the ion-implant energy of 53 KeV by 10 KeV yields 5 times rise in g_m (see Fig. 9.1). Enhancing it by means of

CBL deserves further study.

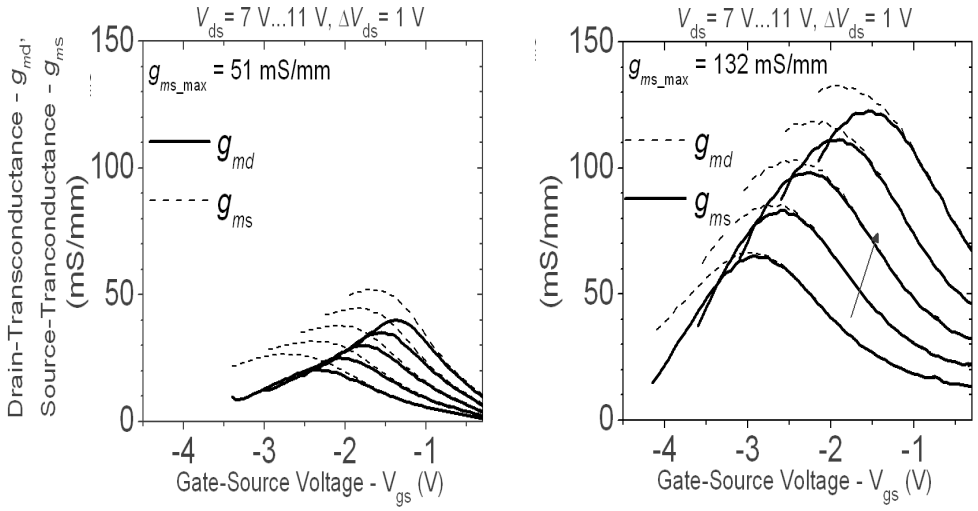


Figure 9.1: g_m vs. VGS traces are shown for a BAVET with (a) 53 KeV and (b) 63 KeV ion implanted CBL. Between (a) and (b) maximum g_m changes from 51 to 132 mS.mm^{-1}. CBL design serves as an effective design methodology for high g_m.

9.1.2 Reducing Gate leakage

Gate leakage is one of the breakdown-limiting factor in a BAVET. Using p-doping for InAlAs had little effect on reducing leakage. For instance, p-doped diodes were found to suffer from more leakage than those with i- or p-i-InAlAs in the low gate-drain voltage regime (see Fig. 9.2). This hinted that leakage in a BAVET might be a combination of factors like a low barrier in the bulk as well as sidewalls of InAlAs. Employing dielectric gate barrier layer is likely a way ahead to addressing the challenge of gate leakage.

9.1.3 A Non-Zero Turn-On Voltage

Turn-on voltage is another parameter critical to transistor's performance, especially power dissipation in a BAVET and also represents certain properties of WBI like barrierof

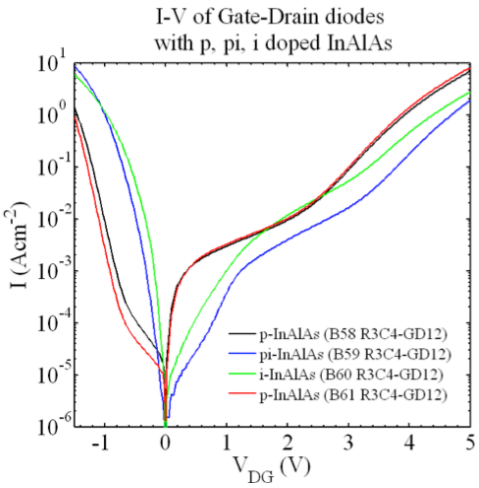
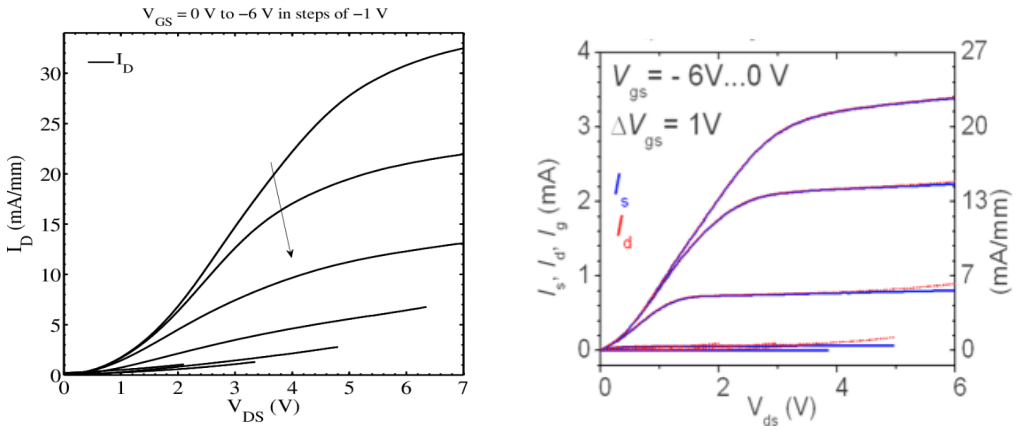


Figure 9.2: Gate-drain leakage characteristics are shown for different doping schemes of the InAlAs gate layer. These devices comprise of InAlAs, InGaAs and aperture–containing III-N layers, with gate formed to InAlAs and the drain to a GaN layer. In low reverse voltage regimes between 0 V to 2 V, p-InAlAs diodes are most leaky, whereas leakage is lowest in 0 V to −1 V. High reverse leakage for p-InAlAs diodes is likely due to their sidewall being unfavorably more conductive than those in i- or p-i-InAlAs diodes.

anInGaAs/III-N junction. The dissertation finds that the barrier can be regulated by the polarization charge of the InGaAs-interfacing III-N layer. The proof of which is shown in Fig. 9.3 wherein by changing the Indium composition of III-N layer from 10% to zero eliminates the turn-on voltage of WBIand BAVET. Polarization of III-N thus provides an interesting performance knob that can be further explored in III-N-based wafer-bonded devices.

9.1.4 Making InGaAs/III-N Junction trap-free

The role of hydrogen in passivation of traps can be further studied to completely eliminate trap activity at WBI. Layer structure using InAlAs doping and polarization of III-N does effect the hydrogen migration and passivation. It will be interesting to study the impact of injecting hydrogen into the bonding chamber while the process of wafer bonding happens. Future investigations may also employ other passivating agents like



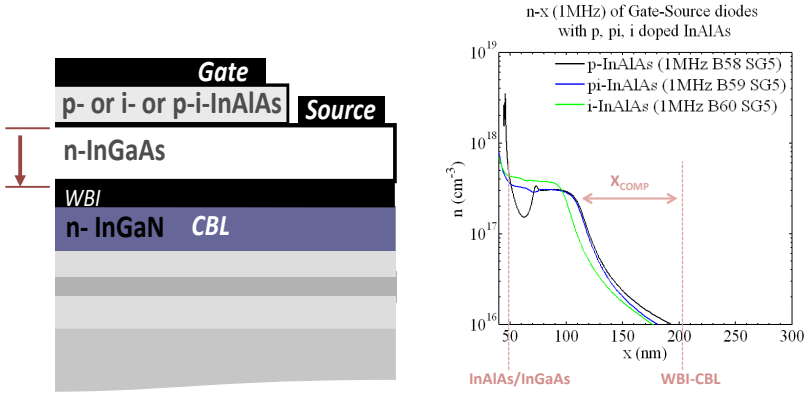
(a) (b)

Figure 9.3: ID, IS vs. VDS characteristics are shown for (a) an InGaN and (b) a GaN BAVET, wherein the WBI comprises InGaAs-InGaN and InGaAs-GaN junctions, respectively. The turn-on voltage reduces if GaN layer replaces InGaN.

oxygen, nitrogen.

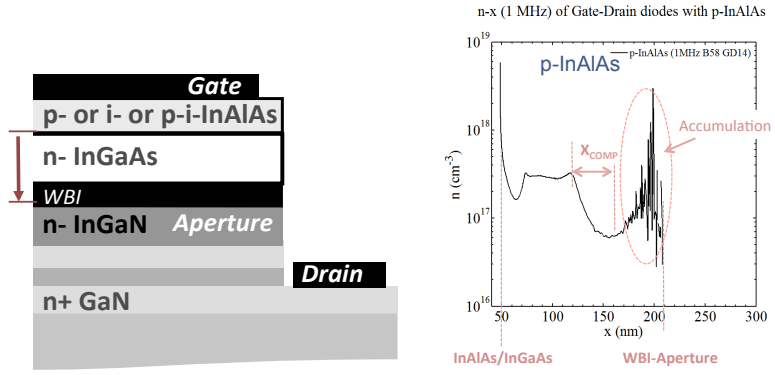
9.1.5 Band Profiling of InGaAs/III-N Junction

An accurate knowledge of band diagrams of novel wafer-heterojunctions is useful to designing semiconductor devices. In this effort, the dissertation has been successful in deducing charge profile at the junction. The information has been revealed through C-V measurements of the heterojunction in CBL and aperture regions. The former's charge profile reveals the effect of compensation of dopants while for the latter a combined compensation and hint of electron accumulation in InGaAs is observed (see Fig. 9.4 and 9.5). With InGaN as a wider bandgap material than InGaAs, an electron accumulation is expected. A further reduction of trap activity is needed to extend the charge profile measurement to InGaN regions and so obtain a band diagram of the WBI.



(a) (b)

Figure 9.4: A cross section schematic of diodes referred to as gate-source diodes is shown. Gate electrode can be formed to a doped InAlAs whereas the second electrode is made to InGaAs layer. WBI represents the interface between InGaAs and CBL-InGaN. Three types of diodes differing in InAlAs doping are characterized for C-V measurements and the charge profile (n) in InGaAs and near WBI regions is derived as shown in (b). Near WBI-CBL regions in n vs. depth (x) profiling show similarity for the three diodes in that their charge profiles shows compensation of dopants. The region of compensation extends along xCOMP.



(a) (b)

Figure 9.5: A cross section schematic of diodes referred to as gate-drain diodes is shown. Gate electrode can be formed to a p-doped InAlAs whereas the second electrode is made to GaN layer. WBI represents the interface between InGaAs and aperture-InGaN. n vs. x profile in InGaAs and near WBI regions is derived as shown in (b). It presents compensation over xCOMP in bulk of InGaAs channel and an accumulation of electrons in region of InGaAs next to WBI. The result reports a partial InGaAs-InGaN heterojunction charge profile which needs further investigation to generate an accurate band diagram.

9.1.6 Integrating Other Materials

The work on III-As/III-N transistors has gained us a knowledge base in bonding process, methods of trap passivation, current blocking layer designs, fabrication processes and device physics that can be generally applied to wafer-bonded devices. All these aspects make us ready to explore bonded transistor designs that are based in other material systems. Towards ultra-high f_t and breakdown, the following materials choices can be extensively explored, GaAs instead of InGaAs, whereas oxide or diamond material systems in place of III-Nitride.

Appendix A

Drain Resistance at Wafer-Bonded Interface

A.1 Introduction

The interface or junction created between materials stacked by wafer-bonding is becoming an extensive part in different semiconductor device designs, both photonics and electronics. Despite using wafer bonding with an intent of combining the physical advantages of different material systems, the anomalous nature of wafer-bonded interface (WBI) has presented limitations to the device performance refs. [1], [2], [3]. A lack of knowledge concerning the junction's electronic properties can thus be an impediment to the development of wafer-bonded junctions, especially in electronic devices. For example, the role of WBI on the operation and performance of an InGaAs/InGaN transistor, referred to a BAVET in ref. [1], needs to be understood in order to realize them as a high frequency power transistor. Herein, we present new experimental findings on the properties of WBI derived in context of a BAVET.

From ref. [1] we understand that the dimension of the gate electrode in a BAVET

can be extended over the aperture regions to result in a redistribution of electrostatic field. The impact can be studied in the changes that L_{GA} brings to the I_{D}-V_{DS} trace.

While ref. [1] has already reported on the L_{GA}-dependent off-state characteristics of BAVETs, this work investigates on how L_{GA} influences their on-state performance. In particular, saturation voltage ($V_{\mathrm{DS\_SAT}}$) of BAVETs is studied as a function of L_{GA}.

The explanation of the correlation between $V_{\mathrm{DS\_SAT}}$ and L_{GA} brings out a significant characteristics pertaining to BAVETs. First of all, increasing L_{GA} adds a drain resistor in the transistor's conduction path. The impact of L_{GA} when studied on BAVETs with different gate potentials reveals the second feature that behavior of WBI is embodied in a response of a resistor.

The study then digresses from the analysis of $V_{\mathrm{DS\_SAT}}$ to understanding the properties of this resistance. While investigating the emergent resistance's relationship to the doping in InAlAs, it is shown that the latter is an effective means to control the conductivity of WBI and aperture. The nature of virtual gate, a phenomenon previously deduced in ref. [4], is presented as well, but for the case of BAVETs that differ in L_{GA}.

A.2 Experiment

Herein, an experiment is conducted that modifies BAVET in its gate design. It is extended to overlap with the aperture. L_{GA} in Fig. A.1 denotes the gate extension performed from either side of an aperture region, which is defined by dimension L_{AP} in Fig. A.1. This is achieved in a manner similar to that of ref. [1], wherein the metallization to create a gate in the CBL regions is applied as well to the aperture regions. Fig. A.1 illustrates the two regions by L_{GO} and L_{GA} dimensions. A complete fabrication process of BAVETs has been elaborated in ref. [5].

With the aim of understanding how the change of electrostatics by L_{GA} influences

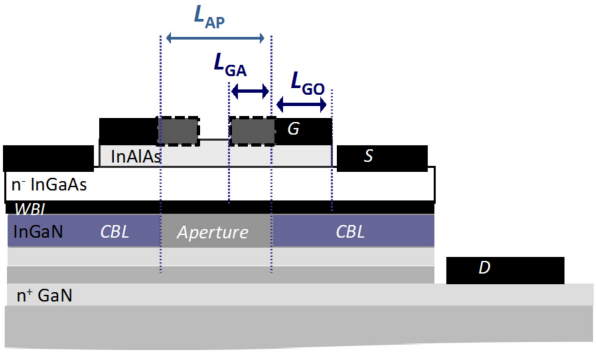


Figure A.1: A cross sectional schematic of a BAVET in which its L_{GA}, L_{GO} and L_{AP} dimensions are defined. L_{GA} and L_{GO} portions of the gate modulate those regions of channel that overlay the aperture and CBL, respectively. An L_{GA} of 0 implies that there is no overlap between the gate and aperture, while a complete overlap in the L_{AP} regions occurs for an L_{GA} equivalent to L_{GA_MAX}. The doping in InAlAs differentiates i,p-i, and p-BAVETs. WBI is the interface between InGaAs and InGaN, which in the aperture regions can be investigated through L_{GA}.

transistor behavior, we restrict to choosing two extremes for the L_{GA} dimension. It may be either 0 or L_{GA_MAX}, the latter is equivalent to half of L_{AP} (see Fig. A.1) [1].

In a latter part of study, L_{GA} variations are applied to three different types of BAVETs. InAlAs layer doping is the differentiating factor (see Fig. A.1). The three BAVETs are referred to as i-, p-i-, and p-BAVETs. InAlAs is doped unintentionally for i-BAVETs while the other two comprise p-doping in their InAlAs layers. The doping is uniformly p-type for the total of InAlAs thickness in a p-BAVET, but for a p-i-BAVET, the thickness is split into two regions of p- and unintentional-doping. Further details on the design of i, p-i and p-BAVETs can be found in ref. [4].

A.3 Analysis Approach

A.3.1 Medians of BAVET Parameters for different L_{GA}

As a first step to analyzing V_{DS_SAT} vs. L_{GA}, we derive medians of different transistor parameters using statistic. We utilize the analysis process described in steps (i)-(v) of

ref. [4].

With $V_{GS} = 0$ V and -2 V, I_D-V_{DS} traces are measured for two sets of BAVETs, wherein each set is linked to an L_{GA}. Different parameters, like V_{DS_SAT}, turn-on voltage: V_{DS_ON}, on resistance: R_{ON}, and maximum on-state current: I_{D_MAX}, result from linearly fitting the I_D-V_{DS} traces. Next step in the analysis is to apply box-plot statistics on parameters of each set. In this way we obtain a median of the parameter that corresponds to an L_{GA}. On obtaining the medians of different parameters, they can be used to regenerate an I_D-V_{DS} representation that depicts the behavior of BAVETs with same L_{GA}.

There are a few devices, especially for i-BAVETs, that are unable to saturate in the voltage range permissible by the parameter analyzer. In such a case, I_D-V_{DS} of the saturation regime does not offer sufficient data points to allow linear fitting. The parameter analyzer imposes a voltage limit at 20 V and because in this limit, saturation is not fully attained, we can only estimate a range for V_{DS_SAT} of such devices. It is said to lie within a range of 15 V – 25 V.

A.3.2 Omission of V_{DS_ON} from I_D-V_{DS}

Ref. [4] also presented a method to calculate an I_D-V_{DS} trace comprising linear and saturation regimes. A similar I_D-V_{DS} trace is derived herein. It requires subtracting V_{DS_ON} from V_{DS}, which also modifies V_{DS_SAT} by the same amount to produce a voltage parameter referred to as V_{KNEE}. I_D can be obtained by dividing the adjusted V_{DS} by R_{ON}. In tracing this as a function of V_{DS}, we are led to the linear regime of I_D-V_{DS}. V_{KNEE}, which marks the end of linear regime, is also the onset of saturation. For the analysis of V_{DS_SAT}, I_D in saturation regime is set to a constant value of I_{D_MAX}. An ideal saturation regime is permissible if the following two conditions are met [4]. Firstly, V_{DS_ON} should be less than both V_{DS_SAT} and V_{KNEE}; secondly a change in output conductance (G_{OUT})

should not influence V_{DS_SAT} [4].

A.4 V_{DS_SAT} vs. L_{GA}

In order to re-evaluate I_D-V_{DS} trace, one needs to first verify whether the two conditions of V_{DS_ON} and G_{OUT} for the saturation regime are supported.

A.4.1 V_{DS_ON} and its dependence on L_{GA}

V_{DS_ON}, or in other words its box-plot median, is estimated to be 2.8 V for i-BAVETs. And with regards to the variation in L_{GA}, V_{DS_ON} changes insignificantly. V_{DS_SAT} is approximated to be in the range of 15 V to 25 V for an I_D-V_{DS} trace measured at V_{GS} = 0 V.

V_{DS_SAT} contains a similar relationship to V_{DS_ON} as it did in ref. [4], which appears herein under the circumstances of variable L_{GA} rather than InAlAs doping. V_{KNEE}, and not V_{DS_ON}, is found to be (a) the primary component of V_{DS_SAT}, and (b) the means by which V_{DS_SAT} can undergo a significant change from one L_{GA} to another.

A.4.2 G_{OUT} and its dependence on L_{GA}

Linear fitting when applied to the saturation regime provides us with a slope equivalent to G_{OUT}. For i-BAVETs, G_{OUT} is extracted from an I_D-V_{DS} trace that sufficiently saturates and enables linear fitting. A trace measured at V_{GS} = - 2 V shows current saturation and is thus well suited for the purpose.

Box-plot G_{OUT} corresponds to medians of 5.57 and 4.47 mS.mm^{-1} for L_{GA} of 0 and L_{GA_MAX}, respectively. We rule out the possibility that L_{GA} controls V_{DS_SAT} through G_{OUT} on the basis that G_{OUT} stays nearly unaffected by L_{GA}.

A.4.3 Re-evaluated I_D-V_{DS} for different L_{GA}

With V_{DS_ON} and G_{OUT} independent of V_{DS_SAT}, both parameters are made zero and a new I_D-V_{DS} trace from V_{KNEE} and R_{ON} is realized. Fig. A.2(a) presents I_D-V_{DS} traces measured for i-BAVETs employing two different L_{GA}. These are on-state traces derived for a V_{GS} of 0 V.

Fig. A.2(a) shows that L_{GA_MAX} certainly causes a higher R_{ON} in i-BAVETs. This is indicative of a collapse in I_D at a given V_{DS}. However, in the absence of current saturation, a question is raised on whether V_{KNEE} increases or decrease due to the behavior of R_{ON}. As V_{KNEE} equals the product of I_{D_MAX} and R_{ON}, the answer may be determined in studying the influence L_{GA} has on I_{D_MAX}.

A.4.4 V_{KNEE} and its dependence on L_{GA}

Fig. A.2(b) presents traces for i-BAVETs when biased at V_{GS} = -2 V. These I_D-V_{DS} traces are of particular interest to this study as they show characteristics of current saturation within the V_{DS} limit of the parameter analyzer. Consequently, the results of I_{D_MAX} and V_{KNEE} vs. L_{GA} are made available.

A comparison of traces in Fig. A.2(b) suggests key information about BAVETs with either L_{GA}. Despite the drain-current collapse, both the device types are able to saturate for the same I_{D_MAX} but at the expense of a shift in V_{KNEE}. The case of L_{GA}-enhanced R_{ON} for V_{GS} = 0 V (see Fig. A.2(a)) reappears for V_{GS} = -2 V (see Fig. A.2(b)). This makes the parameter R_{ON} solely responsible for the incremental impact of L_{GA} on V_{KNEE}.

From Fig. A.2(b) one can deduce the impact of L_{GA} by the following relation on V_{KNEE}:

$$V_{KNEE} = (V_{GS} - V_{TH,DRAIN} + V_X) \tag{A.1}$$

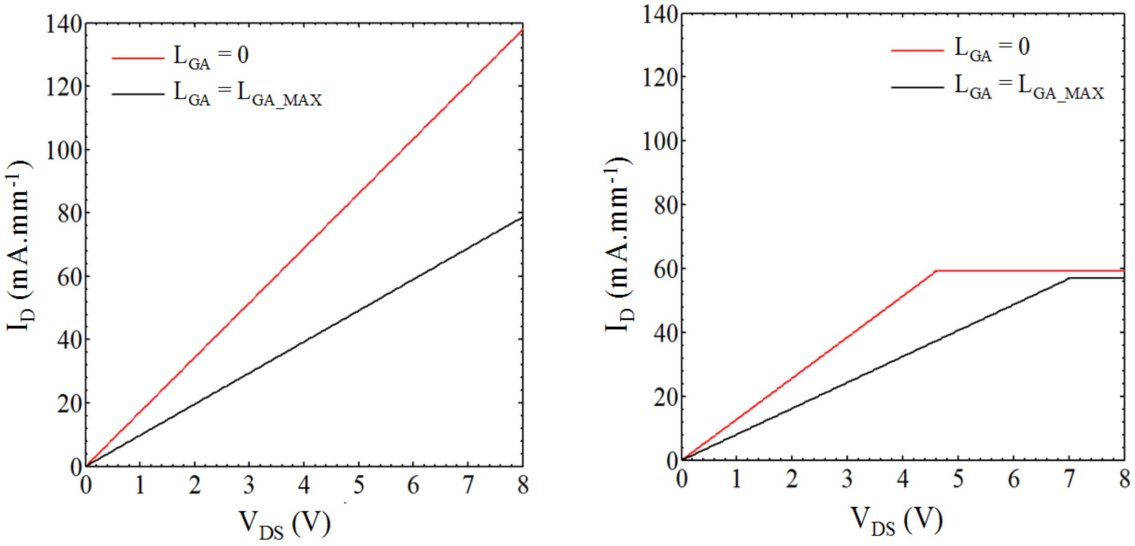


Figure A.2: I_D-V_{DS} traces of i-BAVETs are shown for V_{GS} of (a) 0 V and (b) −2 V. In both (a) and (b), there are two traces for two different L_{GA}, with highest R_{ON} depicted for $L_{\mathrm{GA}} = L_{\mathrm{GA\_MAX}}$.

wherein,

$$V_{\mathrm{X}} = I_{\mathrm{D\_MAX}} \times R_{\mathrm{X}} \tag{A.2}$$

The first term in (A.1) depends on V_{GS} and threshold voltage at drain - $V_{\mathrm{TH,DRAIN}}$, which is the CBL-Aperture edge of the channel [4]. V_{X} is the additional drain voltage and R_{X} is the difference in R_{ON} under the condition that L_{GA} changes from 0 to $L_{\mathrm{GA\_MAX}}$. For i-BAVETs, this change in L_{GA} raises V_{X} as well as R_{X} from zero to a maximum value.

A.5 R_{X}: A Source or Drain Resistance?

With the knowledge that R_{X} originates in the conduction path and is dependent on L_{GA}, there are only three possibilities on where it is located: channel in L_{GO}, or L_{GA} regions; or the region containing WBI-aperture. The conductivity of drift region, a region

buried between the WBI and drain-electrode, is assumed to be independent of L_{GA} and is thus not studied herein. In ref. [4], we illustrated R_{ON} to be a series combination of the resistances in the source and drain regions of the channel, WBI and drift regions. They are referred to as $R_{CH,LGO}$, $R_{CH,LAP}$, $R_{WBI,LAP}$, and R_{DRIFT}. R_X can be found by studying all, but R_{DRIFT}, for a relationship with L_{GA}.

A.5.1 R_X as a Source Resistance?

$R_{CH,LGO}$ becomes the point of investigation to check for R_X as an L_{GA}-enhanced source resistance. In Fig. A.2(b), V_{GS} fixed at -2 V for both L_{GA}. As I_{D_MAX} is not changing, it is implied that $V_{TH,DRAIN}$ is unchanged by L_{GA}. Moreover, in the absence of on-state impact-ionization, threshold voltage at the source assumes the same relationship with L_{GA} as does $V_{TH,DRAIN}$ [4]. How L_{GA} varies thus becomes inconsequential to the conductivity of the channel at both the source and drain edges of L_{GO}. For this reason and that by which V_{KNEE} adjusts without a change in V_{GS} or threshold voltage, we are led to believe that R_X does not arise in L_{GO} region and is not a source resistance. It is instead a drain resistance in BAVETs, which is made dominant with the aid of L_{GA}. The phenomenon, of V_{KNEE} increasing through R_{ON} but not I_{D_MAX}, is similar to what is observed in FETs employing a Schottky contact for the drain electrode [6].

Studying BAVETs with different L_{GA} has pointed out the presence of a parasitic drain resistance, which has an adverse impact on R_{ON}, and V_{KNEE}. In the next section we investigate to find the key feature of the device which gives rise to this parasitic effect.

A.6 R_X: A Resistance in Channel or WBI Regions of Aperture?

In BAVETs, drain resistance can emerge in the channel or WBI regions of aperture. We may next consider $R_{CH,LAP}$ or $R_{WBI,LAP}$ as the possible candidates. The results of varying L_{GA} in i-BAVETs are insufficient to determine which one of the two resistances contributes to R_X. However, we are assured that in extending the gate by L_{GA_MAX}, one enables gate-modulation of the aperture. Both $R_{CH,LAP}$ and $R_{WBI,LAP}$ can thus be impacted.

A.6.1 Methodology

Gate-modulation works on varying the gate potential by V_{GS} or surface potential of the gate. Gate-potential is another degree of freedom that can be of use in differentiating between the two resistors. To this end, we perform another experiment wherein devices differ in gate potential.

We briefly introduce the steps to find R_X by gate-potential experiment. The influence of L_{GA} on R_X may change in devices with different gate potentials. One can anticipate the possible outcomes and express them in form of two boundary conditions. According to whether R_X is $R_{CH,LAP}$ or $R_{WBI,LAP}$, boundary conditions are expected to acquire a different behavior. The experimental results are checked for boundary conditions of one of the resistors - $R_{CH,LAP}$. In the event of a match between its boundary conditions and experimental results, the question of what constitutes R_X is settled on $R_{CH,LAP}$. However, if the experiment behaves contrary, then $R_{WBI,LAP}$ becomes the choice for R_X.

A.6.2 Experiment to Determine If R_{X} is $R_{\mathrm{CH,LAP}}$ or $R_{\mathrm{WBI,LAP}}$

The gate potential is varied by means of employing different surface potential. One way to change the surface potential is to change the doping in the gate layer. Therefore, in conjunction to applying different L_{GA} in devices, the doping of InAlAs layer is also varied.

A.6.3 Doping InAlAs to Vary Gate Potential

The design of i- and p-BAVETs are sufficient to realize two different gate potentials. It is hereinafter referred to as Ψ_{S}. Fig. A.3(a), and (b) show BAVETs comprising unintentionally and p-doped InAlAs, respectively. Built-in voltage extraction from capacitance-voltage measurements (C-V) produces Ψ_{S}. As expected, introduction of p-doping raises the Ψ_{S} from 0.43 to 1.41 V, with the latter equivalent to the energy bandgap of InAlAs. The respective surface potentials are denoted by $\Psi_{\mathrm{S,i}}$ and $\Psi_{\mathrm{S,p}}$ in the band diagrams shown in Fig. A.3(c), and (d). In comparison to i-BAVETs, a higher Ψ_{S} in p-BAVETs results in a larger depletion width of the channel.

A.6.4 $R_{\mathrm{CH,LGO}}$ as a Function of Gate Potential

Let us first consider i- and p-BAVETs with $L_{\mathrm{GA}} = 0$ μm. For a fixed V_{GS} but different Ψ_{S}, $R_{\mathrm{CH,LGO}}$ will differ in its magnitude for the two BAVETs. We recall ref. [4], which established this difference to be on account of the varying depletion charge profiles. Thus, was observed a higher $R_{\mathrm{CH,LGO}}$ in p-BAVETs than i-BAVETs. Fig. A.4 shows resistors of different magnitudes placed in L_{GO} regions of i- and p-BAVETs. From an earlier argument on L_{GA}-dependent drain resistance, it is proposed that irrespective of what is chosen for L_{GA}, $R_{\mathrm{CH,LGO}}$ changes with Ψ_{S} in a similar fashion. But this characteristic may not be true for $R_{\mathrm{CH,LAP}}$ and $R_{\mathrm{WBI,LAP}}$ as we will see in a latter section.

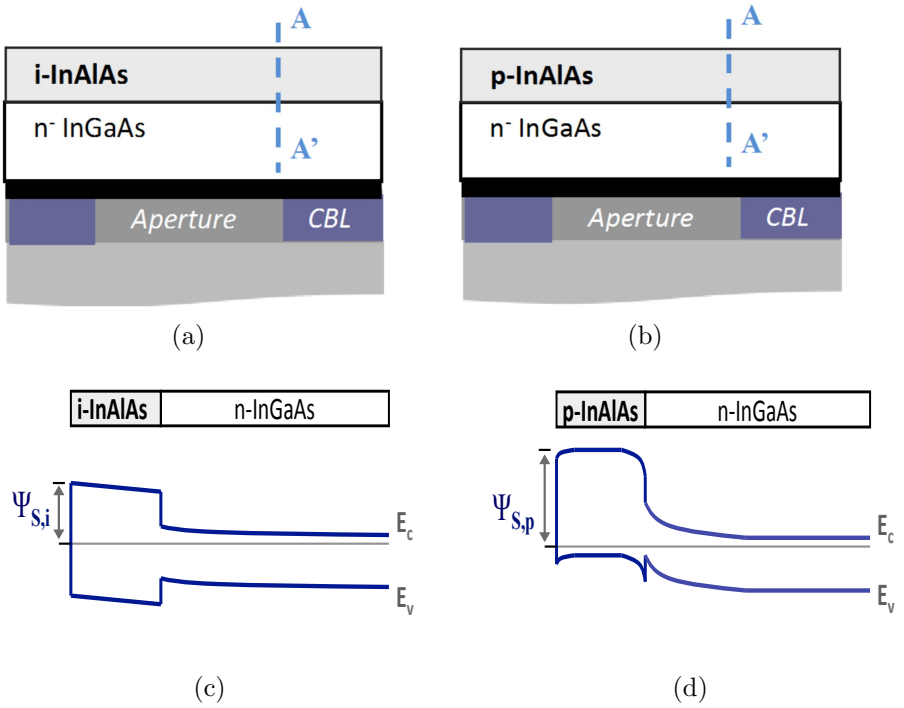


Figure A.3: Layer structures showing different doping in InAlAs for (a) i-, and (b) p-BAVETs Energy band diagrams along A-A' are shown for (c) i- and (d) p-BAVETs under equilibrium conditions. E_C and E_V denote the conduction and valence band edges. Ψ_S is the surface potential which is the difference in the surface Fermi-pinning and the surface conduction band edge. At equilibrium, Ψ_S is proportional to the built-in potential of InAlAs/InGaAs junction and depletion region width of the InGaAs layer. p-BAVETs are associated with a higher Ψ_S.

A.6.5 $R_{CH,LAP}$ as a Function of Gate Potential

Ψ_S increases $R_{CH,LAP}$ by the same principle that influenced $R_{CH,LGO}$. Fig. A.5 compares i- and p-BAVETs in their different $R_{CH,LAP}$.

A.6.6 $R_{WBI,LAP}$ as a Function of Gate Potential

The presence of electrically-active traps at WBI prevent an accurate extraction of charge profile and the resultant electrostatics. As part of another ongoing study it has been observed that the behavior of traps can change with Ψ_S through a mechanism

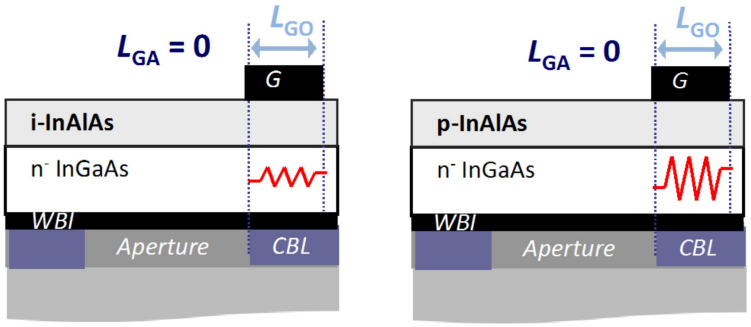


Figure A.4: (a) An i-BAVET showing one half of the device with a gate in L_{GO} regions. There is no overlap between the gate and aperture. $R_{CH,LGO}$ is denoted by a resistor. (b) A similar schematic showing $R_{CH,LGO}$ for p-BAVETs. The resistivity of L_{GO} regions of the channel is implied by the size of the resistor. A larger sized resistor is placed in p-BAVETs than in i-BAVETs to signify higher resistivity of the former.

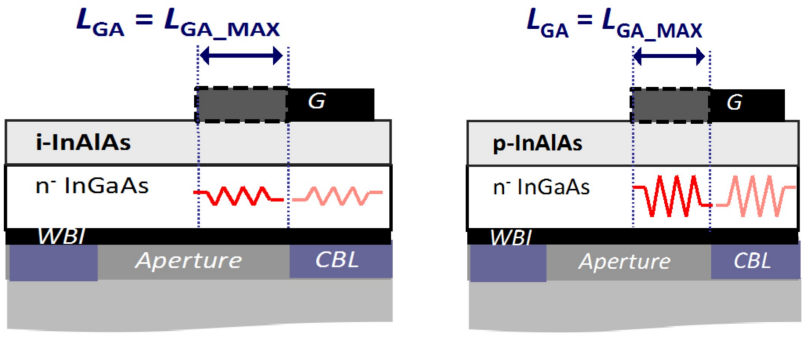
of passivation. Deriving $R_{\mathrm{WBI,LAP}}$ vs. Ψ_{S} is thus not as straightforward as it is for $R_{\mathrm{CH,LGO}}$ and $R_{\mathrm{CH,LAP}}$. However, we attempt to deduce its behavior in a latter section by understanding R_{X} vs. Ψ_{S}.

A.7 R_{X} vs. Gate Potential

We proceed in finding whether R_{X} is $R_{\mathrm{CH,LAP}}$ or $R_{\mathrm{WBI,LAP}}$ from the relationship of R_{X} and Ψ_{S}. R_{X} is recalled from an earlier secton to be an L_{GA}-induced change in R_{ON}, or ΔR_{ON}. In studying R_{X} vs. Ψ_{S}, the impact of L_{GA} is inherent in the definition of R_{X}.

A.7.1 Boundary Conditions for R_{X}

Two boundary conditions, namely BC#1 and BC#2 are formulated to identify R_{X}. In BC#1: R_{X}, for any Ψ_{S}, can be either greater than or equal to zero. A negative R_{X} is not considered a valid case of BC#1 for reasons that are described as follows. Negative R_{X} is representative of R_{ON} reducing for an increase in L_{GA}. This is an unlikely situation



(a) (b)

Figure A.5: (a) An i-BAVET showing one half of the device with a gate extended over the aperture regions by a dimension of $L_{\mathrm{GA\_MAX}}$. Besides $R_{CH,LGO}$ in the L_{GO} regions, there is an additional resistor - $R_{CH,LAP}$ - in the channel's aperture region. (b) A similar schematic showing $R_{CH,LGO}$ and $R_{CH,LAP}$ for p-BAVETs. The difference in $R_{CH,LAP}$ of the two BAVETs is represented by the different sizes of their resistors.

due to the absence of impact-ionization in the on-state regime for either of the L_{GA} [4].

BC#2 identifies the trend followed by R_{X} for a given change in Ψ_{S}. Specifically, R_{X} may exhibit a positive or a negative coefficient with Ψ_{S}.

The above mentioned conditions are expected hold different values based on whether R_{X} is related to $R_{\mathrm{CH,LAP}}$ or $R_{\mathrm{WBI,LAP}}$. In the following section, we report these values for the case that R_{X} is an L_{GA}-controlled $R_{\mathrm{CH,LAP}}$.

A.7.2 Boundary conditions if R_{X} is $R_{\mathrm{CH,LAP}}$

Unlike $R_{\mathrm{CH,LGO}}$, which is only a function of Ψ_{S}, $R_{\mathrm{CH,LAP}}$ depends on both Ψ_{S} and L_{GA}. $R_{\mathrm{CH,LAP}}$, which is the channel resistor in the L_{AP} regions, will increase with L_{GA} in a similar way as the channel resistance increases with gate-length in a field-effect transistor. R_{ON} may then change, as a function of L_{GA}, through $R_{\mathrm{CH,LAP}}$ and the change is reflected in R_{X} becoming greater than zero.

R_{X} may behave such for both i- and p-BAVETs. But their different $R_{\mathrm{CH,LAP}}$ will lead to R_{X} of different magnitudes. By this argument, we should expect R_{X} to be much

higher in p-BAVETs than in i-BAVETs in the case that R_{X} is due to $R_{\mathrm{CH,LAP}}$. This means that R_{X} may demonstrate a positive coefficient with Ψ_{S}.

The two boundary conditions associated with R_{X} as $R_{\mathrm{CH,LAP}}$ can be stated to be valid in the following forms. BC#1 holds true when R_{X} is greater than zero in both i- and p-BAVETs. While for the other condition, R_{X} must increase when going from i- to p-BAVETs.

We next check for these boundary conditions in the available experimental data on i- and p-BAVETs. And if it follows that data does not meet the boundary conditions then one can deduce that $R_{\mathrm{CH,LAP}}$ is not the basis of R_{X}.

A.7.3 L_{GA} dependence of I_{D}-V_{DS} in p-BAVETs

p-BAVETs with different L_{GA} are characterized for their I_{D}-V_{DS} responses. The process of re-evaluating I_{D}-V_{DS} is repeated to remove the turn-on regime. It is mentioned that for p-BAVETs $V_{\mathrm{DS\_ON}}$ is not changed by L_{GA}, and in this particular respect they are similar to i-BAVETs. Fig. A.6 presents the re-evaluated I_{D}-V_{DS} for the two L_{GA} dimensions. In response to different L_{GA}, I_{D}-V_{DS} is impacted in neither R_{ON} nor V_{KNEE}. The constant nature of R_{ON} results in an R_{X} of zero. This is in contrast to how i-BAVETs responded to L_{GA}. As can be seen in Fig. A.3, R_{X} is greater than zero in i-BAVETs for the reason that L_{GA} enhances R_{ON}.

A.7.4 Proof of R_{X} as a resistance at WBI

As R_{X} is greater than zero for i-BAVETs but equals zero for p-BAVETs, BC#1 is said to possess different outcomes for different Ψ_{S}. Only i-BAVETs meet the criteria of BC#1 for $R_{\mathrm{CH,LAP}}$. p-BAVETs do not show any sign of $R_{\mathrm{CH,LAP}}$ getting enhanced with L_{GA}. Thus, we encounter the first instance indicating the resistor, which impacts

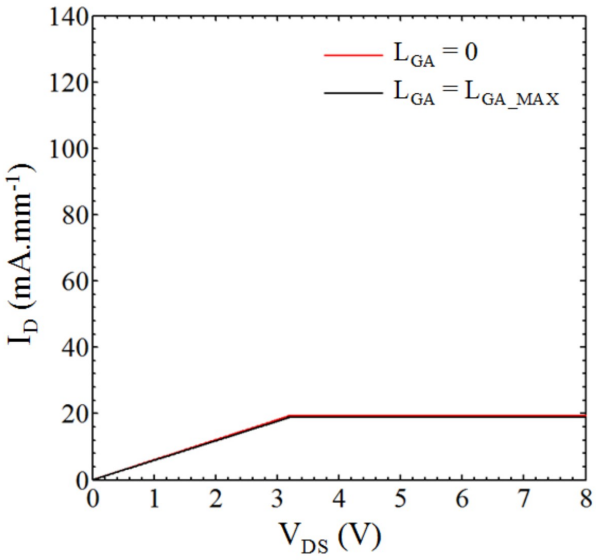


Figure A.6: I_D-V_{DS} traces measured at V_{GS} of -2 V for p-BAVETs with two different L_{GA}. The measurement is done at V_{GS} of -2 V. Unlike i-BAVETs in Fig. A.3; p-BAVETs with different L_{GA} are similar in their R_{ON} and V_{KNEE}.

i-BAVETs, but not p-BAVETs, may not be $R_{CH,LAP}$.

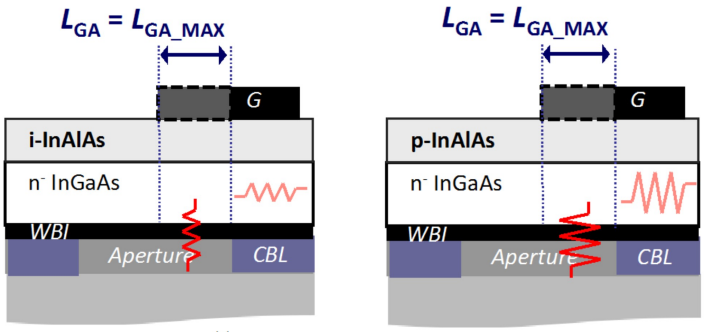
R_X in p-BAVETs is less than that in i-BAVETs, an inequality interpreted as larger the Ψ_S, smaller the R_X. The relationship furnishes us the second boundary condition in that R_X is experimentally shown to have a negative coefficient with Ψ_S. This again opposes the nature of $R_{CH,LAP}$ through BC#2.

Had R_X been associated with $R_{CH,LAP}$, one would expect these experimentally realized boundary conditions to conform to those derived by theoretical means. But as the expectation is not met for either of the boundary conditions pertaining to $R_{CH,LAP}$, the argument that R_X originates in $R_{CH,LAP}$ is hence disproved. Because $R_{CH,LGO}$ and $R_{CH,LAP}$ do not alter R_X, the drain resistance must come about due to $R_{WBI,LAP}$.

A.7.5 Explanation of R_X vs. Ψ_S

The difference in R_X of i- and p-BAVETs is the difference in the magnitude of their $R_{WBI,LAP}$. Ψ_S impacts R_X through $R_{WBI,LAP}$, specifically $R_{WBI,LAP}$ reduces when Ψ_S

increases. (see Fig. A.7). We base this phenomenon on a hypothesis that the electrostatic-field changes by L_{GA} impact WBI of i-BAVETs to a greater degree by than they do so for p-BAVETs. It is the nature of WBI that has changed with Ψ_S.



(a) (b)

Figure A.7: (a) An i-BAVET showing one half of the device with a gate extended over the aperture regions by a dimension of L_{GA_MAX}. Besides $R_{CH,LGO}$ in the L_{GO} regions, there is an additional resistor – $R_{WBI,LAP}$ - in the WBI-aperture region. (b) A similar schematic showing $R_{CH,LGO}$ and $R_{WBI,LAP}$ for p-BAVETs. The difference in $R_{WBI,LAP}$ of the two BAVETs is represented by the different sizes of their resistors; larger the size, higher the $R_{WBI,LAP}$.

A.8 A Method To Eliminate R_X

A.8.1 $R_{WBI,LAP}$ and Aperture Conductivity

WBI is the top interface of aperture region (see Fig. A.1) and in this way aperture conductivity is made a function of $R_{WBI,LAP}$. The results of $R_{WBI,LAP}$ vs. Ψ_S indicate that aperture conductivity incrseases with the latter. Highly conductive apertures are offered in p-BAVETs. In this section we intend to confirm this role of Ψ_S, or doping in InAlAs, on aperture conductivity. It is done so by investigating a third type of BAVETs - p-i-BAVETs. They are characterized, re-evaluated for I_D-V_{DS} and compared for different L_{GA}. The comparison leads us to R_X for p-i-BAVETs.

A.8.2 On How to Control $R_{\mathrm{WBI,LAP}}$

In tracing R_{X} for different Ψ_{S}, p-i-BAVET fall in the range of that of i- and p-BAVETs (see Fig. A.8(a)). Both R_{X} and V_{X} steadily decrease from an i-BAVET to a p-BAVET, through p-i-BAVET (see Fig. A.8). Evidence confirms a new phenomenon, wherein one can control aperture conductivity in a region close to the InGaAs/InGaN WBI by the choice of the doping employed in the layer of InAlAs.

A.8.3 Traps at WBI

Wafer bonding of highly lattice-mismatched semiconductors, such as InGaAs and InGaN, is expected to result in a WBI with traps that are electrically-active [7], [8]. R_{WBI} is one of the metrics to evaluate trap-related electronic behavior of a WBI. A favorable elimination of $R_{\mathrm{WBI,LAP}}$ in BAVETs with p-doped InAlAs is suggestive of mitigated trap activity at WBI. Trap activity among the three BAVETs reduces in the same order, as does $R_{\mathrm{WBI,LAP}}$.

Further understanding on the trap behavior for different InAlAs doping is needed. But from another study investigating passivation of traps, Ψ_{S} is suspected to be a factor that determines the trap passivation of WBI and thus controls trap activity.

A.9 Properties of $R_{\mathrm{WBI,LAP}}$

The following discussion illustrates few chief properties of $R_{\mathrm{WBI,LAP}}$. It depends on two physical parameters: L_{GA} and doping in InAlAs. The dependence comes about by the following two mechanisms: redistribution of electrostatic field in the aperture - which is performed by L_{GA}; and controlling the activity of traps that is made feasible through the choice of doping.

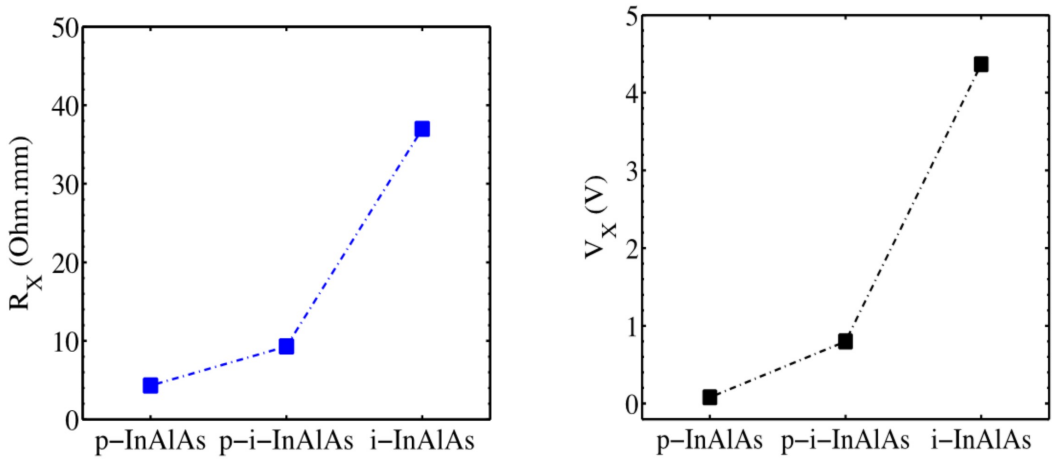


Figure A.8: (a) R_{X}, and (b) V_{X} vs. InAlAs doping. R_{X} and V_{X} for each InAlAs doping are box plot medians derived for respective BAVETs. These are measured at V_{GS} = -1 V. Among the three types of BAVETs, i-BAVETs exhibit highest R_{X} and V_{X}.

Experimental results show that the two properties are related to each other. A formulation of relationship is offered in that $R_{\mathrm{WBI,LAP}}$ is made more sensitive to changes in electric field when there are electrically active traps present at the WBI. For i- and p-i- BAVETs, which are adversely impacted by trap activity, this rule is experimentally observed. The lower electric field, the higher is $R_{\mathrm{WBI,LAP}}$. Moreover, in the case of p-BAVETs, reduced trap activity results in an $R_{\mathrm{WBI,LAP}}$ that is either eliminated or made insensitive to L_{GA}-induced changes in electrostatic field.

A.10 Virtual Gate in BAVETs With $L_{\mathrm{GA\_MAX}}$

In this section we return to an earlier idea of virtual gate [4]. In ref. [4], focus was laid on understanding $V_{\mathrm{DS\_SAT}}$ in BAVETs for different InAlAs. It should be recalled that the phenomenon of virtual gate was derived when L_{GA} = 0 μm in BAVETs. Another aspect of the analysis was that virtual gate was derived for the case of $I_{\mathrm{D\_MAX}}$ increasing

without a change in R_{ON}. The situation was opposite to what has been highlighted in the present study wherein $I_{\mathrm{D\_MAX}}$ remains fixed despite the change in R_{ON} - a phenomenon identified as drain-resistance effect.

$I_{\mathrm{D\_MAX}}$ not changing with L_{GA} is a clear evidence that virtual gate has not changed with L_{GA}. If it is assumed that virtual gate and drain-resistance are not interdependent, then in removing the drain resistance, or the corresponding V_{X}, we essentially remove the L_{GA} dependence from BAVETs. The result of this is that, firstly $V_{\mathrm{DS\_SAT}}$ for the case of $L_{\mathrm{GA\_MAX}}$ is similar to that shown in ref. [4], wherein L_{GA} was 0. Secondly, BAVETs with $L_{\mathrm{GA\_MAX}}$ show a dependency of $V_{\mathrm{DS\_SAT}}$ on InAlAs doping which is identical to that of ref. [4]. One can then argue that virtual gate may exist in BAVETs with $L_{\mathrm{GA\_MAX}}$ as they do in those with no L_{GA}.

A.11 Conclusion

L_{GA} extension of the gate electrode in i-BAVETs was shown to have incremental effects on V_{KNEE} and R_{ON}. An explanation was availed in parallelism drawn with drain resistance of FETs. In increasing L_{GA} in BAVETs, a parasitic drain resistance of R_{X} was introduced. The voltage absorbed by R_{X} amounted to the voltage by which V_{KNEE} increases as a function of L_{GA}.

The investigation then focused on finding the part of the conduction path contributing to this resistance. Between $R_{\mathrm{CH,LGO}}$, $R_{\mathrm{CH,LAP}}$ and $R_{\mathrm{WBI,LAP}}$, we succeeded in eliminating the first two as the possible factors by means of two experiments. The constant nature of $I_{\mathrm{D\_MAX}}$ for different L_{GA} supported the argument of R_{X} being unrelated to $R_{\mathrm{CH,LGO}}$. For the role of $R_{\mathrm{CH,LAP}}$ in inducing R_{X}, two boundary conditions were formulated and checked for in i- and p-BAVETs. The test of the boundary conditions yielded results contrary to expectations, and thus challenged the likelihood that R_{X} appeared as $R_{\mathrm{CH,LAP}}$. By the

process of elimination of $R_{\mathrm{CH,LGO}}$ and $R_{\mathrm{CH,LAP}}$, $R_{\mathrm{WBI,LAP}}$ was revealed to be the drain resistance in question. The same resistance also leads to the anomalous factor of V_{X} in V_{KNEE}.

Had it not been for the gate-potential affecting the boundary conditions of $R_{\mathrm{CH,LAP}}$ and $R_{\mathrm{WBI,LAP}}$ in different ways, it would have been difficult to recognize R_{X} as $R_{\mathrm{WBI,LAP}}$. The experimental approach can be a method determining the resistance of a WBI.

Reducing L_{GA} in i- and p-i-BAVETs reduces the impact of $R_{\mathrm{WBI,LAP}}$. L_{GA} dependence was made non-existent by using p-doping for the entirety of InAlAs thickness in BAVETs. Studying the impact of L_{GA} in conjunction to InAlAs doping variations thus addressed another significant aspect that $R_{\mathrm{WBI,LAP}}$ can be controlled in BAVETs. And as $R_{\mathrm{WBI,LAP}}$ represents aperture conductivity, the latter can be influenced as well. A hypothesis was proposed that links the control mechanism to the behavior of traps at WBI. On the basis of which it was stated that the presence of traps is the reason for L_{GA} dependence observed in BAVETs. Mitigating traps is the way to reducing $R_{\mathrm{WBI,LAP}}$.

In general, BAVETs can be impacted in their V_{KNEE} through two parasitic effects, namely virtual gate and drain resistance. Both of which can be overcome by the method of p-doping in gate-barrier layer.

Further studies are needed to accurately model resistance and distribution of electrostatic field in the aperture regions of the channel, and WBI. One of the studies on $R_{\mathrm{WBI,LAP}}$ in devices with different aperture widths is presently ongoing and will be presented in a future work. Additionally, breakdown in BAVETs with different L_{GA} needs to be reviewed as we expect drain resistance to influence the breakdown. How doping the gate barrier impacts passivation of traps at WBI is an interesting phenomenon that, too, will be presented in a future study.

However, this study has succeeded in answering the following questions: (a) Which one of the factors, resistance or threshold voltage, makes $V_{\mathrm{DS\_SAT}}$ high as L_{GA} is increased?

Resistance. (b) Where does the additional factor of on-resistance arise in the device, whether it is in the channel or aperture? It is the region of WBI sandwiched between channel and aperture. (c) What mechanism explains relationship between resistance of WBI with electrostatic field and gate-barrier doping? The impact arises in both modifying the activity of traps at WBI.

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Appendix B

Higher Gate-Aperture Overlap for Improved Pinch-off

B.1 Introduction

A transistor design aimed at achieving power-switching operation at high frequencies was developed in the form of a Bonded Aperture Vertical Electron Transistor (BAVET) (see Fig. B.1) [1]. The design is based on a current aperture vertical electron transistor (CAVET) in which the drain-layer is buried underneath the channel region [2, 3]. Using the technique of wafer-bonding in a CAVET enables integration of epitaxially distinct material systems for the channel and drift-regions. Thus, the advantages offered by the physical properties of two material-systems can be favorably adopted into a wafer-bonded transistor. In this work, an $In_{0.53}Ga_{0.47}As$ (InGaAs) channel and a III-Nitride (III-N) based drift-region are chosen to simultaneously achieve a high-injection velocity (injection velocity $\simeq 2.75 \times 10^7$ cm/sec for InGaAs field-effect transistors) and a high-breakdown voltage (breakdown-field for GaN = 3.3 MV/cm) (see Fig. B.1(a)) [4, 5].

Current-conduction in a BAVET is due to the electrons initially flowing laterally along

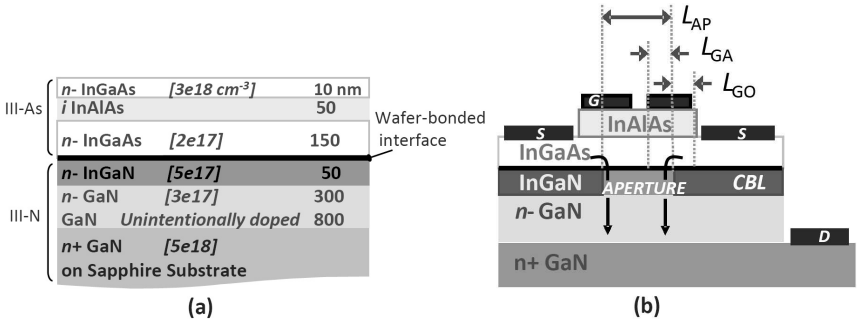

Figure B.1: (a) Layer structure of a BAVET showing the n-doping concentration and thickness of each layer. (b) Cross-sectional schematic of a BAVET with the gate, source, and drain electrodes marked by G, S, and D, respectively. Electron-conduction in the device is shown by solid arrows. The specified dimensions are the aperture length (L_{AP}), gate-CBL overlap (L_{GO}), and gate-aperture overlap (L_{GA}).

the InGaAs channel, and then vertically through the III-N drift-region (see Fig. B.1(b)). In the III-N region, ion-implanted current-blocking regions (referred to as current-blocking-layer or CBL) confine the current path to a narrow conductive region called the aperture (defined by L_{AP} in Fig. B.1(b)). In addition to isolating the current-path, the CBL also acts as a back-barrier for the InGaAs channel. Owing to the vertical topology of the device, the gate-electrode can be lithographically defined such that it controls the charge in two regions of the InGaAs channel, wherein one part of the gate-dimension overlaps with the CBL-region (L_{GO}) and the remainder overlaps with the aperture-region (L_{GA}) (see Fig. B.1(b)). The L_{GO} dimension enforces channel-modulation, and the L_{GA} controls the electric-field profile in the vicinity of the aperture-CBL edge, and thus, functions as a field-plate. We investigate herein the factors impacting the channel-pinch-off by studying its dependence on the L_{GO} and L_{GA} dimensions.

B.2 Device Design

The wafer-bonded interface of the III-Arsenide (III-As)/III-N BAVET presented herein is formed between InGaAs and $In_{0.1}Ga_{0.9}N$ (InGaN) layers. InGaN interlayer is added to

reduce the conduction-band barrier to the electrons transiting from the InGaAs channel to GaN [1]. The aperture region is defined in the InGaN layer. The ion-implantation process for forming the CBL regions employs an [Al] dose of 10^{15} cm^{-2} and ion-implant energy of 53 keV. A Schottky-type gate-electrode to the $In_{0.52}Al_{0.48}As$ (InAlAs) layer is formed after etching the InGaAs cap layer. The source and drain contacts are deposited on the InGaAs channel, and n-GaN layers, respectively. The device design and fabrication process has been previously reported in [1]. For the three-terminal measurements, all three currents: drain- (I_D), source- (I_S), and gate-current (I_G) are recorded. As will be shown in the next section, the presence of high gate-drain leakage (I_{GD}) makes it necessary to study the channel-pinch-off behavior using the I_S characteristics.

B.3 Results and Discussion

The DC I_D-V_{DS} characteristics of a BAVET with $L_{GO} = 1$ μm and $L_{GA} = 0$ μm are shown in Fig. B.2(a). The two factors impacting the off-state performance in this device are the weak gate-control on the channel and high I_G (both I_{GD} and gate-source leakage - I_{GS}) (see Fig. B.2(b)). This letter focuses on understanding the factors behind the weak gate-control observed in I_S by comparing the off-state behavior of BAVETs with different L_{GO} and L_{GA}.

To investigate the role of drain-induced barrier lowering (DIBL) on gate-modulation, three BAVETs with different L_{GO} but same channel-thickness (referred to as t) and L_{GA} are fabricated. Fig. B.2(c) compares the logarithmic traces of I_S-V_{DS} characteristics of these three BAVETs, wherein the applied V_{GS} is varied from -6 V to -4 V. In this regime of V_{GS}, gate-modulation in I_S is independent of the L_{GO}/t ratio which eliminates DIBL as the cause of weak pinch-off in I_S.

Another possible phenomenon impacting the gate-control is the occurrence of break-

down in the device. Using a gate-connected field-plate (denoted by L_{GA} in Fig. B.1(b)) is a useful means to understand the off-state behavior as it redistributes the peak electrostatic fields in the channel, consequently influencing the breakdown in the device. The Drain-Current-Injection method (DCIM) is used to distinguish between gate- or/and channel-related breakdown in BAVETs with different L_{GA} but fixed L_{GO} [6]. In this method, I_S, I_G, and V_{DS} are monitored while injecting a fixed I_D of 3.3 mA/mm and ramping down V_{GS} towards pinch-off.

In this paragraph, DCIM measurements are briefly explained using the V_{DS}, I_S, and I_G characteristics of a BAVET with $L_{GA} = L_{GA\_MAX}$ wherein $L_{GA\_MAX} = 0.5 \times L_{AP}$ (see Fig. B.3). The V_{DS}-V_{GS} trace exhibits two regimes namely I and II marked by the transition voltages: V_{GS_T1} and V_{GS_T2} (see Fig. B.3(a)). As V_{GS} is ramped down in regime I ($V_{GS\_T2} \leq V_{GS} \leq V_{GS\_T1}$), I_S drops from 3.3 mA/mm at $V_{GS} = V_{GS\_T1}$ to $I_S \simeq 0$ mA/mm at $V_{GS} = V_{TH}$ (see Fig. B.3(b)). Maintaining $I_D = 3.3$ mA/mm while I_S decreases requires an increase in I_G such that $I_G = I_D - I_S$ which is achieved with a sharp rise in V_{DS} as the applied V_{GS} is made more negative (see Fig. B.3(c), and (a)). ΔV_{BDS} is the maximum increase in V_{DS} measured at $V_{GS} = V_{GS\_T2}$. In Fig. B.3(a) V_{DS} reaches its peak value when channel pinch-off is achieved ($I_S \simeq 0$ mA/mm in Fig. B.3(b)). Applying V_{GS} beyond pinch-off reduces V_{DS} with V_{GS} at a slope $\simeq 1$ to maintain a constant V_{GD}, and hence a constant $I_{GD} \simeq I_D = 3.3$ mA/mm while both I_{GS} and I_S remain negligible (see Fig. B.3(a)). The peak V_{DS} then denotes the breakdown voltage (referred to as BV_{DS}) of the device, and for $L_{GA} = L_{GA\_MAX}$ it is limited by gate-breakdown. A BV_{DS} and ΔV_{BDS} of 4 V and 1.8 V, respectively are obtained for $L_{GA} = L_{GA\_MAX}$ (see Fig. B.3(a)).

On comparing the I_S-V_{GS} characteristics for different L_{GA}, V_{TH} becomes more negative as L_{GA} is reduced, suggesting diminished gate-control as field-plating decreases (see Fig. B.3(b)). Furthermore, for a given V_{GS}, the slope of I_G-V_{GS} trace decreases with

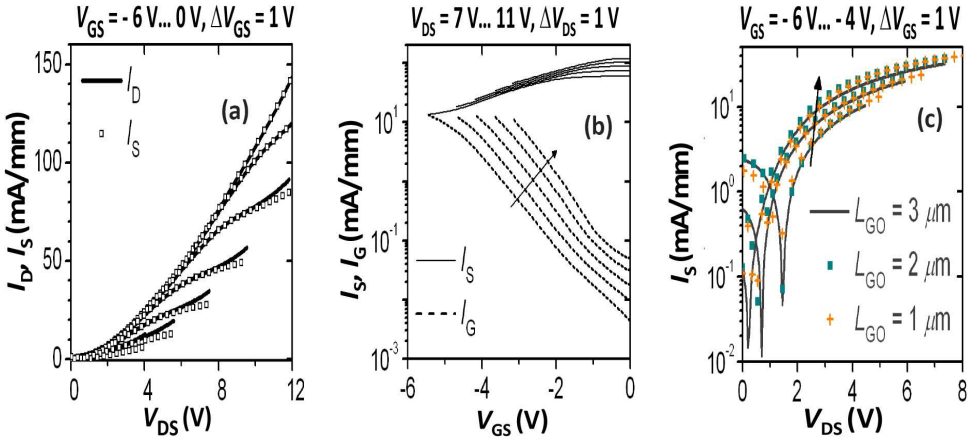

Figure B.2: (a) I_{D}, I_{S}-V_{DS}, and (b) I_{S}, I_{G}-V_{GS} for a BAVET with $L_{\mathrm{AP}} = 10$ μm, $L_{\mathrm{GO}} = 1$ μm, and $L_{\mathrm{GA}} = 0$ μm. (c) Comparison of I_{S}-V_{DS} for BAVETs with $L_{\mathrm{GO}} =$ 3, 2, and 1 μm when measured in the pinch-off regime of -6 V $\leq V_{\mathrm{GS}} \leq$ -4 V. For the three devices, $t = 150$ nm, $L_{\mathrm{AP}} = 4$ μm, and $L_{\mathrm{GA}} = 0$ μm.

L_{GA} and the lowest I_{G} is obtained when $L_{\mathrm{GA}} = 0$ μm (see Fig. B.3(c)). Lower I_{G} but weaker pinch-off as L_{GA} reduces is an indicator of channel-breakdown rather than gate-breakdown limiting the ability to pinch-off the channel. Additionally, the dependence of gate-control on the field-plate strongly suggests that this channel-breakdown is caused by impact-ionization. The peak electrostatic-field at the gate-drain edge of the channel is higher in the absence of field-plate ($L_{\mathrm{GA}} = 0$ μm) which unfavorably triggers impact ionization.

The following sections discuss the effect of impact-ionization on the electrostatic-field distributions at the gate-source and gate-drain edges of a device with $L_{\mathrm{GA}} = 0$ μm (see Fig. B.4(a)). The holes generated by impact-ionization in the channel can either flow to the gate- or the source-electrodes depending on the gate-channel or source-drain electrostatic-fields, respectively. Due to the valence-band discontinuity of 0.2 eV at the InGaAs/InAlAs interface, only a small fraction of the holes is collected by the gate, and majority of them travel to the gate-source edge of the channel (see Fig. B.4(b)) [7]. The holes then accumulate at the gate-source edge which is the most negative

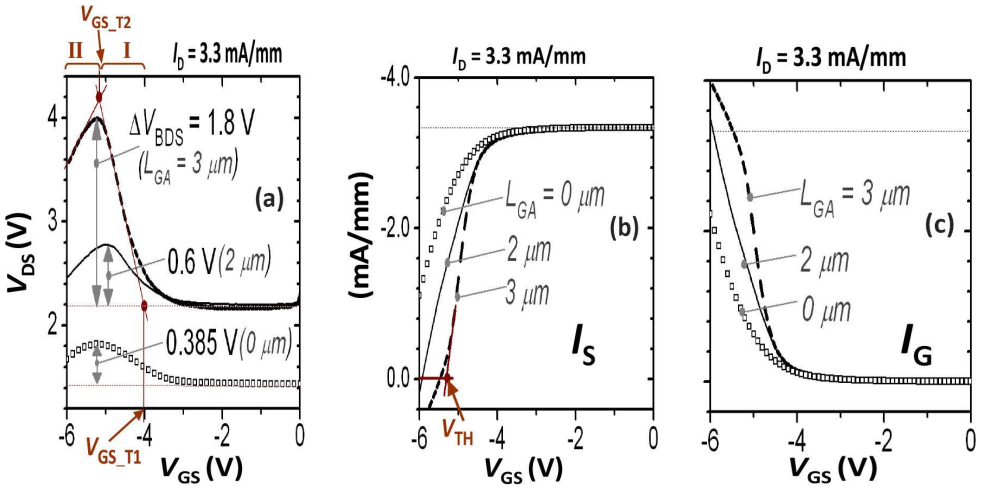

Figure B.3: DCIM measurements for I_{D} = 3.3 mA/mm on BAVETs with different L_{GA} ($L_{\mathrm{GA\_MAX}}$ = 3 μm, 2 μm, and 0 μm), but similar L_{AP} = 6 μm, and L_{GO} = 1 μm: (a) V_{DS}-V_{GS}, (b) I_{S}-V_{GS}, and (c) I_{G}-V_{GS}. The transition voltages $V_{\mathrm{GS\_T1}}$, and $V_{\mathrm{GS\_T2}}$, mark the two regimes: regime I and II, respectively. ΔV_{BDS} is shown for each L_{GA}. V_{TH} is the V_{GS} at which $I_{\mathrm{S}} \simeq 0$ mA/mm.

potential region of the channel and modulate both the vertical and lateral electrostatic-fields (see Fig. B.4(b)). For a given V_{GS}, accumulation of holes increases the electrostatic field across the gate-barrier while the channel-potential (referred to Ψ) becomes more positive. This change in Ψ reduces the barrier to electrons flowing from source to drain and enhances the off-state I_{S} which increases V_{TH} in a way similar to the kink-effect observed in SOI MOSFETs [8].

DCIM measurement allows V_{DS} to set up such that $I_{\mathrm{G}} = I_{\mathrm{D}} - I_{\mathrm{S}}$ is maintained. Increase in I_{S} due to impact-ionization for $L_{\mathrm{GA}} = 0$ μm can be viewed as an enhancement in channel-conductivity. Under these conditions, maintaining I_{D} then requires a reduction in V_{DS}. In a BAVET, a part of V_{DS} is contributed by the channel potential at the gate-drain edge (V_{CH}). For a given V_{GS}, a change in V_{CH} alters the gate-channel potential ($V_{\mathrm{G\_CH}} = V_{\mathrm{GS}} - V_{\mathrm{CH}}$), and consequently determines I_{G}. This is illustrated in Fig. B.4(c), wherein the reduction in V_{CH} (denoted by ΔV_{CH}) decreases the electrostatic potential sustained across the gate-barrier by ΔV_{B}. Thus, both ΔV_{BDS} and I_{G} reduce

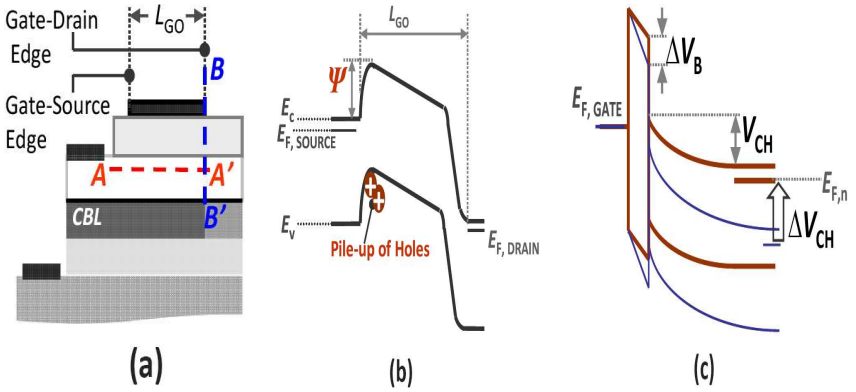

Figure B.4: (a) A cross-sectional schematic of the L_{GO} section of a BAVET when $L_{GA} = 0$ μm, and dotted lines denoting the gate-source- and gate-drain edges of the channel. For a given V_{GS} in regime I of DCIM measurements: (b) energy-band-profile along *AA'* in the channel shows the accumulation of holes at the gate-source edge. Ψ is the conduction-band barrier which controls I_S. (c) Band-diagram along *BB'* at the gate-drain edge shows the change in band-diagram caused by impact-ionization, wherein ΔV_{CH} and ΔV_B are the reduction in channel potential (V_{CH}) and gate potential, respectively.

as L_{GA} is decreased (see Fig. B.3(a) and (c)).

Reduction in V_{CH} creates a negative-feedback to impact-ionization which limits carrier-multiplication, and results in a softer channel-pinch-off instead of an abrupt breakdown in devices with $L_{GA} < L_{GA\_MAX}$. However, by using $L_{GA} = L_{GA\_MAX}$, the field-plate effect is used to mitigate impact-ionization (see Fig. B.3). The improvement in the channel pinch-off for this field-plate design is evident from the I_S-V_{DS} and I_S-V_{GS} characteristics of the transistor (see Fig. B.5). A maximum I_D of 192 mA/mm and an extrinsic transconductance of 55 mS/mm are measured at $V_{DS} = 11$ V. Improving pinch-off in I_D by reducing I_G will be addressed in a future study.

In conclusion, the study of comparing the off-characteristics for different gate and field-plate dimensions has shown that channel-impact-ionization primarily prevents pinch-off in BAVETs. The method of using L_{GA} as a gate-connected field-plate eliminates channel-breakdown, improves channel-pinch-off and is found to be a key design feature in improving the off-state performance of BAVETs.

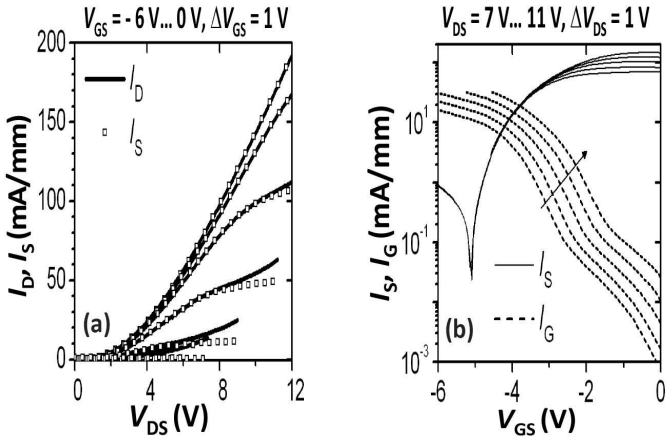

Figure B.5: (a) I_{D} , I_{S}-V_{DS} and (b) I_{S}, I_{G}-V_{GS} measurements on a BAVET with $L_{\mathrm{AP}} = 8$ μm, $L_{\mathrm{GO}} = 1$ μm, and $L_{\mathrm{GA}} = L_{\mathrm{GA\_MAX}}$.

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